Nos. 22-1465, -1466, -1467, -1549, -1550, -1551, -1552 (consolidated)

United States Court of Appeals for the Federal Circuit

Nos. 2022-1465, -1466, -1467

ARBOR GLOBAL STRATEGIES, LLC, *Appellant*,

v.

SAMSUNG ELECTRONICS CO., LTD.,
TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD., *Appellees*,

KATHERINE K. VIDAL, Under Secretary of Commerce for Intellectual Property and Director of the U.S. Patent & Trademark Office, *Intervenor*.

Appeals from U.S. Patent & Trademark Office, Patent Trial & Appeal Board, Nos. IPR2020-01020, IPR2020-01021, and IPR2020-01022.

Nos. 2022-1549, -1550, -1551, -1552

ARBOR GLOBAL STRATEGIES, LLC, *Appellant*,

v.

XILINX, INC., TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD., *Appellees*,

KATHERINE K. VIDAL, Under Secretary of Commerce for Intellectual Property and Director of the U.S. Patent & Trademark Office, *Intervenor*.

Appeals from U.S. Patent & Trademark Office, Patent Trial & Appeal Board, Nos. IPR2020-01567, IPR2020-01568, IPR2020-01570, and IPR2020-01571

APPELLEES' RESPONSE BRIEF

James M. Glass
Eric Huang
QUINN EMANUEL URQUHART & SULLIVAN, LLP
51 Madison Avenue
New York, NY 10010
(212) 849-7000

for Taiwan Semiconductor Mfg. Co., Ltd.

Jeffrey Shneidman
FISH & RICHARDSON P.C.
One Marina Park Drive
Boston, MA 02210
(617) 542-5070

John Dragseth
FISH & RICHARDSON P.C.
60 S. Sixth St., Ste 3200
Minneapolis MN 55402
(612) 335-5070

for Xilinx, Inc.

John C. O'Quinn
F. Christopher Mizzo
William H. Burgess
KIRKLAND & ELLIS LLP
Washington, DC 20005
202-879-5000

Meredith Zinanni
KIRKLAND & ELLIS LLP
300 North LaSalle
Chicago, IL 60654
(312) 862-2000

for Samsung Electronics Co., Ltd.

Additional counsel on inside-front cover

March 1, 2023

David M. Hoffman
Kenneth Darby
FISH & RICHARDSON P.C.
111 Congress Ave., Suite 810
Austin TX 78701
(512) 472-5070

for Xilinx, Inc.

U.S. Patent No. 6,781,226, claim 13 (Appx700)

13. A processor module comprising:
at least a first integrated circuit die element including a programmable array;
at least a second integrated circuit die element including a processor stacked with and electrically coupled to said programmable array of said first integrated circuit die element;
at least a third integrated circuit die element including a memory stacked with and electrically coupled to said programmable array and said processor of said first and second integrated circuit die elements respectively; and
means for reconfiguring the programmable array within one clock cycle.

U.S. Patent No. RE42,035, claim 1 (Appx688)

1. A processor module comprising:
at least a first integrated circuit die element including a programmable array;
at least a second integrated circuit die element stacked with and electrically coupled to said programmable array of said first integrated circuit die element; and
wherein said first and second integrated circuit die elements are electrically coupled by a number of contact points distributed throughout the surfaces of said die elements, and wherein said contact points traverse said die elements through a thickness thereof.

CERTIFICATE OF INTEREST
(Samsung)

Counsel for Appellee Samsung Electronics Co., Ltd. certify the following:

1. Represented Entities (Fed. Cir. R. 47.4(a)(1)): Samsung Electronics Co., Ltd.

2. Real Party in Interest (Fed. Cir. R. 47.4(a)(2)): Samsung Electronics America, Inc.; Samsung Semiconductor, Inc.

3. Parent Corporations and Stockholders (Fed. Cir. R. 47.4(a)(3)): N/A.

4. Legal Representatives (Fed. Cir. R. 47.4(a)(4)):

Kirkland & Ellis LLP: Bao Nguyen; Gregory S. Arovas

5. Related Cases (Fed. Cir. R. 47.4(a)(5), 47.5(b)):

Arbor Global Strategies, LLC v. Samsung Electronics Co., Ltd., et al., No. 2:19-CV-00333-JRG-RSP (E.D. Tex.)

Arbor Global Strategies, LLC v. Xilinx, Inc., No. 1:19-CV-01986-MN (D. Del.)

6. Organizational Victims and Bankruptcy Cases (Fed. R. App. P. 26.1(b)-(c)): N/A.

CERTIFICATE OF INTEREST
(Xilinx)

Counsel for Appellee Xilinx, Inc. certify the following:

1. Represented Entities (Fed. Cir. R. 47.4(a)(1)): Xilinx, Inc.

2. Real Party in Interest (Fed. Cir. R. 47.4(a)(2)): N/A.

3. Parent Corporations and Stockholders (Fed. Cir. R. 47.4(a)(3)): Advanced Micro Devices, Inc.

4. Legal Representatives (Fed. Cir. R. 47.4(a)(4)): N/A.

5. Related Cases (Fed. Cir. R. 47.4(a)(5), 47.5(b)):

Arbor Global Strategies, LLC v. Samsung Electronics Co., Ltd., et al., No. 2:19-CV-00333-JRG-RSP (E.D. Tex.)

Arbor Global Strategies, LLC v. Xilinx, Inc., No. 1:19-CV-01986-MN (D. Del.)

6. Organizational Victims and Bankruptcy Cases (Fed. R. App. P. 26.1(b)-(c)): N/A.

CERTIFICATE OF INTEREST
(TSMC)

Counsel for Appellee Taiwan Semiconductor Manufacturing Company, Ltd. certify the following:

1. Represented Entities (Fed. Cir. R. 47.4(a)(1)): Taiwan Semiconductor Manufacturing Company, Ltd.

2. Real Party in Interest (Fed. Cir. R. 47.4(a)(2)): N/A.

3. Parent Corporations and Stockholders (Fed. Cir. R. 47.4(a)(3)): N/A.

4. Legal Representatives (Fed. Cir. R. 47.4(a)(4)):

Quinn Emanuel Urquhart & Sullivan LLP: Ziyong Li

5. Related Cases (Fed. Cir. R. 47.4(a)(5), 47.5(b)):

Arbor Global Strategies, LLC v. Samsung Electronics Co., Ltd., et al., No. 2:19-CV-00333-JRG-RSP (E.D. Tex.)

Arbor Global Strategies, LLC v. Xilinx, Inc., No. 1:19-CV-01986-MN (D. Del.)

6. Organizational Victims and Bankruptcy Cases (Fed. R. App. P. 26.1(b)-(c)): N/A.

TABLE OF CONTENTS

TABLE OF AUTHORITIES

Cases

Statutes

Other Authorities

STATEMENT OF RELATED CASES

No other appeal from the proceedings below was previously before this or any other appellate court. *Arbor Global Strategies, LLC v. Samsung Electronics Co., Ltd., et al.,* No. 2:19-CV-00333-JRG-RSP (E.D. Tex.), and *Arbor Global Strategies, LLC v. Xilinx, Inc.*, No. 1:19-CV-01986-MN (D. Del.) may directly affect or be directly affected by the Court's decision in this case.

INTRODUCTION

Arbor appeals from seven final written decisions invalidating 107 claims of four patents, most on multiple obviousness grounds. Each decision contains detailed reasoning supported by substantial evidence. Arbor's three arguments on appeal lack merit.

First, for one patent with means-plus-function elements, Arbor contends the Board should have required petitioners to show a single prior-art reference disclosing the corresponding structure and function together. Arbor's arguments misstate the record, misread this Court's decisions, and effectively propose an anticipation case within an obviousness case for means-plus-function elements. Obviousness does not require disclosures of entire claim elements from single prior-art references, for *any* claim. A prior-art *combination* may render claims obvious if the challenger shows that a skilled artisan would combine teachings and reasonably expect success. The Board applied the correct standard, and substantial evidence supports its findings.

Second, Arbor attacks all seven decisions as "tainted by hindsight." Arbor fails to engage with the Board's reasoning or reckon with the substantial-evidence standard. Substantial evidence supports the Board's

findings, and Arbor's "hindsight" refrain merely expresses Arbor's disagreement with the results.

Finally, Arbor asks this Court to overrule or ignore *Ethicon Endo-Surgery, Inc. v. Covidien LP*, 812 F.3d 1023 (Fed. Cir. 2016), and hold that the Board's decisions violate the APA and due process because the same panel rendered the institution and final decisions. *Ethicon* not only binds the panel, it is correct. *Ethicon* explains that institution is adjudicatory, not prosecutorial, and no different from numerous other preliminary decisions that do not make the adjudicator unfit to rule on the ultimate merits—such as a district court issuing a warrant or granting a preliminary injunction, or the Supreme Court granting certiorari.

Ethicon also explains that precedent rejects the foundations of Arbor's "bias" arguments. Arbor contends that, because "[n]obody likes to admit when they are wrong," the final decisions can be dismissed as the APJs "rationaliz[ing]" the institution decisions through "hindsight and confirmation bias." OpeningBr.1-3. But Supreme Court precedent holds that adjudicators are presumed to act with honesty and integrity, and preliminary comments on the merits are not "'bias" or "prejudice." It may

be that "nobody likes to admit when they are wrong," but that would explain Arbor's decision to pursue these appeals, not the Board's rulings invalidating Arbor's patents. This Court should affirm.

STATEMENT OF THE ISSUES

1. Whether obviousness of the '226 patent's means-plus-function claims should be affirmed because the Board applied the correct legal standards, and substantial evidence supports its factual findings.

2. Whether the final written decisions should be affirmed because Arbor's "hindsight" arguments lack merit, and substantial evidence supports the Board's findings.

3. Whether it violates the APA or due process for the same panel of APJs to render the institution decision and final written decision in the same IPR—which this Court held it does not in *Ethicon* and *Mobility Workx*.

STATEMENT OF THE CASE

Arbor appeals from seven final written decisions, invalidating claims of four Arbor patents. *See infra* p.9 (chart). Samsung was the petitioner in three proceedings. Xilinx was the petitioner in four. In all seven proceedings, Taiwan Semiconductor Manufacturing Company

(TSMC) filed parallel petitions and was joined as a petitioner. *E.g.*, Appx1035-1046.

I. Arbor's Challenged Patents

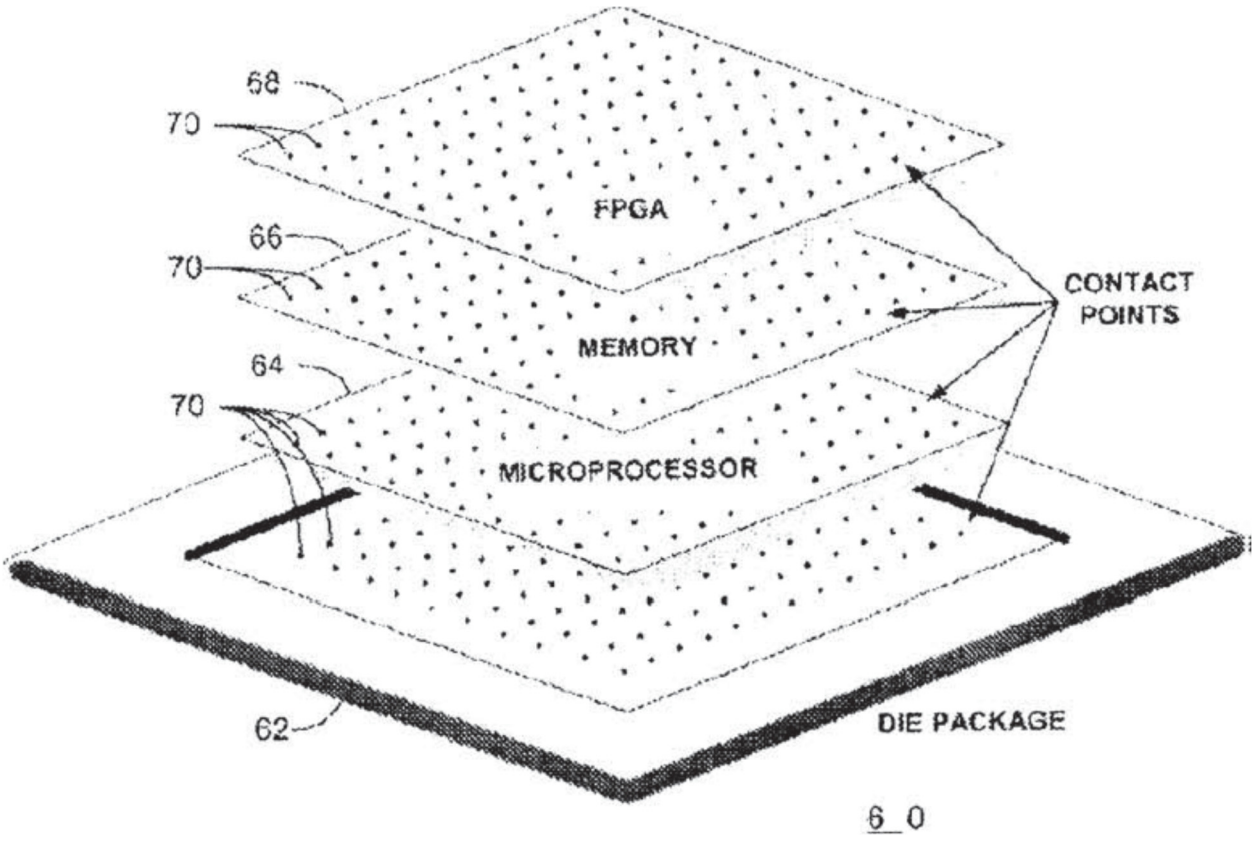
The four challenged Arbor patents—Nos. RE42,035 (Appx680-690), 6,781,226 (Appx691-701), 7,126,214 (Appx702-713), and 7,282,951 (Appx714-725)—are related to each other as continuations or continuations-in-part. Except for the '226 patent's means-plus-function claims, differences between the patents are generally not relevant here.

The specifications all describe Arbor's purported invention as a reconfigurable processor that includes a field-programmable gate array (FPGA) stacked with other components. Appx686(2:9-30). FPGAs are integrated circuits whose logic can be reconfigured, including during operation. FPGAs have been known and used since the 1980s, and—the patents acknowledge—are "typically" incorporated into processors to make the processor reconfigurable. Appx686(1:16-36).

The specifications state that the processor's components are made on thin wafers, stacked vertically, and connected with "metal contacts." Appx686(2:9-30). The "metal contacts can traverse the thickness of the wafer creating small bumps on the back side," creating so-called through-

silicon vias connecting the stacked wafers. *Id.*; Appx1298-1299(¶47). According to the specifications, the stacked configuration permits more connections between components, and the stacking and connections make it possible to reconfigure the processor quickly. *E.g.*, Appx686(2:27-49).

Figure 4 shows an embodiment. FPGA, memory, and microprocessor layers are stacked, and connected by "contact points, or holes," Appx687(4:14) (the dots, 70).



Appx684; Appx687(3:25-28); Appx687-688(3:38-6:9).

The '035 patent's claim 1 is exemplary. It recites a processor with "die elements" (including a "programmable array") that are stacked together and connected to each other by through-silicon vias ("electrically coupled by … contact points [that] traverse said die elements through a thickness thereof"):

> **1.** A processor module comprising:
>
> at least a first integrated circuit die element including a programmable array;
>
> at least a second integrated circuit die element stacked with and electrically coupled to said programmable array of said first integrated circuit die element; and
>
> wherein said first and second integrated circuit die elements are electrically coupled by a number of contact points distributed throughout the surfaces of said die elements, and wherein said contact points traverse said die elements through a thickness thereof.

Appx688.

Relevant to these appeals, the '226 patent's independent claims 13 and 22 include means-plus-function elements. Appx700. Those claims use numerous parallel connections between the memory and FPGA components (*e.g.*, as shown by the dots in Figure 4 above). All of the data needed to reconfigure the FPGA is passed from memory to FPGA simultaneously over those numerous parallel connections, so that the FPGA is

reconfigured in one clock cycle. Thus, the specification states that in an embodiment, the FPGA "may be totally reconfigured in one clock cycle by updating all of the configuration cells in parallel." Appx687(3:29-33, 4:45-47, 4:54-56). And the '226 patent's claims 13 and 22 each recite "means for" either "reconfiguring the programmable array" or "updating the plurality of configuration logic cells," "within one clock cycle":

> **13.** A processor module comprising:
>
> at least a first integrated circuit die element including a programmable array;
>
> at least a second integrated circuit die element including a processor stacked with and electrically coupled to said programmable array of said first integrated circuit die element;
>
> at least a third integrated circuit die element including a memory stacked with and electrically coupled to said programmable array and said processor of said first and second integrated circuit die elements respectively; and
>
> means for reconfiguring the programmable array within one clock cycle.

Appx700.[1]

Under the Board's constructions, which Arbor does not challenge, the corresponding structure for both claims is "*a wide configuration data*

[1] All quoted emphasis is added unless otherwise indicated.

port and contact points formed throughout the area of the first integrated circuit die element and another integrated circuit die element." Appx152-153; Appx541-542. The "wide configuration data port" is "a configuration data port connecting in parallel cells on one die element to cells on another die element." Appx147; Appx537.

II. Samsung, Xilinx, and TSMC File IPR Petitions, Leading to Seven Final Decisions Invalidating All Challenged Claims.

Samsung and Xilinx independently challenged Arbor's patents in *inter partes* reviews, each relying on distinct sets of prior art that disclosed: stacking components (including FPGAs, processors, and memories), connecting stacked components with through-silicon vias, and the benefits of such arrangements. In total, the PTAB found 107 claims of Arbor's patents unpatentable, most on multiple grounds. Some challenged claims were anticipated, and all were obvious. The following chart shows the combined results:

Patent	Petitioner	Unpatentable Claims	Basis (Reference(s))
6,781,226	Samsung	13, 14, 16-23, 25-30	obvious (Koyanagi, Cooke)
		13, 14, 16-23, 25-30	obvious (Bertin, Cooke)
	Xilinx	1-6	obvious (Zavracky, Chiricescu, Akasaka)
		7-12	obvious (Zavracky, Chiricescu, Akasaka, Satoh)
		13-30	obvious (Zavracky, Chiricescu, Aksasaka, Trimberger)
7,282,951	Samsung	1, 4, 5, 8, 10, 13-15	obvious (Koyanagi, Alexander)
		1, 4, 5, 8, 10, 13-15	obvious (Bertin, Cooke)
	Xilinx	1-2, 4-6, 8-24, 27, 29	obvious (Zavracky, Chiricescu, Akasaka)
		25	obvious (Zavracky, Chiricescu, Akasaka, Trimberger)
		26	obvious (Zavracky, Chiricescu, Akasaka, Satoh)
		28	obvious (Zavracky, Chiricescu, Akasaka, Alexander)
RE42,035	Samsung	1, 5, 7	anticipated (Alexander)
		9, 13, 15	obvious (Alexander, Admitted Prior Art)
		1, 3, 5-9, 11, 13-17, 19-22, 25, 26, 28, 29	obvious (Koyanagi, Alexander)
		1, 3, 5-9, 11, 13-17, 19-22, 25, 26, 28, 29	obvious (Bertin, Cooke)
	Xilinx	1-30, 33, 36, 38	obvious (Zavracky, Chiricescu, Akasaka)
		31, 32, 34	obvious (Zavracky, Chiricescu, Akasaka, Trimberger)
		35	obvious (Zavracky, Chiricescu, Akasaka, Satoh)
		37	obvious (Zavracky, Chiricescu, Akasaka, Alexander)
7,126,214	Xilinx	1, 2, 4, 6, 26, 27, 29, 31	obvious (Zavracky, Chiricescu, Akasaka)
		3, 28	obvious (Zavracky, Chiricescu, Akasaka, Satoh)
		5, 30	obvious (Zavracky, Chiricescu, Akasaka, Alexander)

A. Samsung Challenges and Invalidates Claims of the '226, '951, and '035 Patents, Each on Multiple Grounds.

1. Samsung Challenges All Claims as Obvious in Light of Koyanagi (with Alexander or Cooke) and in Light of Bertin (with Cooke).

Samsung's petitions challenged the '035, '226, and '951 patents. *See* Appx734; Appx3802; Appx6513. In addition to arguments Arbor leaves unchallenged on appeal, Samsung contended that all challenged claims are obvious twice-over: in light of **(a)** Koyanagi combined with either Alexander or Cooke, and **(b)** Bertin combined with Cooke.

a. Prior Art

Koyanagi (Appx1844-1849) is a publication describing "*three-dimensional* integration technology" with vertically-stacked chips. Appx1844.[2] Like Arbor's patents, Koyanagi discloses that stacking permits more connections between stacked components—"[m]ore than 10^5 interconnections per chip … in a vertical direction"—which "enable[s] large data bandwidth in vertical data transfer." *Id.* Koyanagi "enables a huge number of metal microbumps to form on the top or bottom surfaces of the chips." Appx1844-1845.

Koyanagi's figures 1(a) and 2 (below) illustrate modules that stack different types of chip dies—such as microprocessors, memory, and a processor array and output circuit.

[2] Samsung presented many of the same exhibits in each IPR. Where the same document appears in multiple IPR records, this brief cites one version to avoid unnecessary duplication in the appendix.

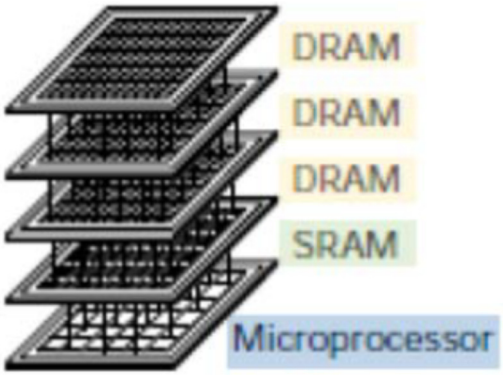


Fig. 1(a) (Appx1845, as highlighted at Appx747)

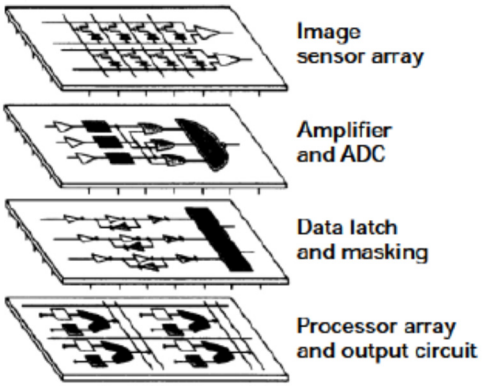


Fig. 2 (Appx1845)

As Samsung's expert explained, Koyanagi's technology did not depend on the type of the dies—*i.e.*, a skilled artisan would recognize that components *other* than those explicitly disclosed could also be stacked with the same technology. Appx1325(¶101); Appx4362(¶75); Appx7122(¶66).

Bertin (Appx1860-1873), like Koyanagi and like Arbor's patents, discloses stacked chip dies and interconnections using through-silicon vias. Bertin describes "the ability to stack similar chips while providing high speed chip-to-chip connections through the silicon." Appx1872(7:16-18). The "high speed chip-to-chip connections" are formed using through-silicon vias (which Bertin calls "through-chip conductors") and distributed chip-to-chip connectors. Appx1872(7:16-34); Appx1312-1313(¶74); Appx4359-4360(¶70); Appx7120(¶61). Both are formed by conventional

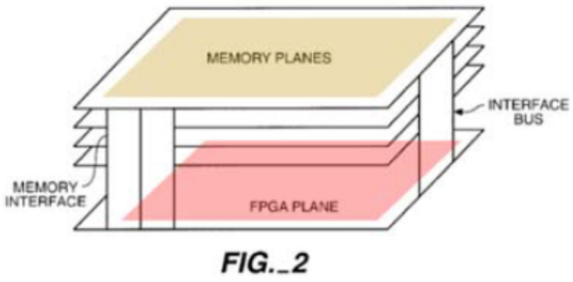
processes, which confirms that Bertin's stacked chips are bare dies, as in Arbor's patents.[3] Bertin's chip-to-chip connections "provide high system packing densities, and … high performance inter-chip and intra-chip communication and heat dissipation," which provides a universal way of interconnecting stacked chips because the connections are designed to "accommodate different chip sizes and structures" and are suitable for use in 3D devices having as many as 20 vertically stacked dies. Appx1869(2:61-65); Appx1871(6:49-51); Appx1872(7:50-55); Appx1313(¶76); Appx4360(¶72); Appx7121(¶63).

Alexander (Appx1840-1843) describes stacked FPGA dies, through-silicon vias, and benefits of both. Appx1840-1843. Alexander describes a "*three-dimensional* (3D) architecture" with stacked "2D FPGA bare dies," that are "interconnected using *solder bumps*" that "establish electrical contacts." Appx1840. Each die "has vias passing through the die itself, enabling electrical interconnections between the two sides of

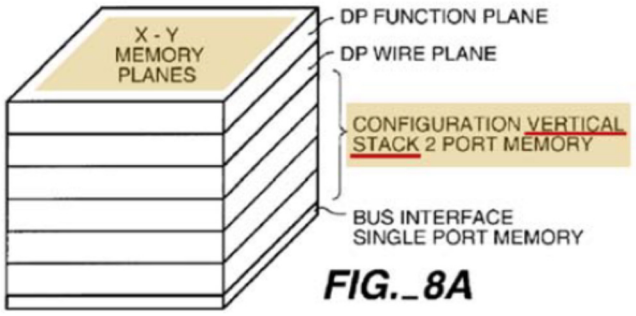
[3] Appx1861-1862(figs. 3-4); Appx1870(3:21-40) (formation of through-chip conductors); Appx1864(fig. 10); Appx1871(5:22-6:5) (formation of chip-to-chip connectors); Appx1313(¶75); Appx4360(¶71); Appx7121(¶62).

the die." *Id.*; Appx1841 (Figure 2). Alexander explains FPGAs "can implement arbitrary logic" and "provide designers with a faster and more economical design cycle." Appx1840.

Cooke (Appx1850-1859) describes a "reconfigurable processor chip," containing "a standard processor, blocks of special FPGA logic, and unique interfaces between them" that provides "the flexibility of software development, with the performance of dedicated hardware solutions." Appx1850; Appx1856(2:3-11). Cooke's Figure 2 includes "memory planes"—described in Figure 8A as a "vertical stack" of configuration memory—stacked over an "FPGA plane."



Appx745 (Appx1851, color added)



Appx745 (Appx1854, color and underlining added)

Cooke teaches that the "configuration memory stack … allow[s] for nearly instantaneous reconfiguration" because "[e]ach FPGA has two or more memory planes which can shift into the FPGA function *in a single cycle*." Appx1850; Appx1856(2:47-49). Samsung's expert explained that loading

configuration data into the FPGA in one clock cycle permits reconfiguration in one clock cycle. Appx7119-7120(¶60); *see also* Appx1307(¶64); Appx4354(¶60).

b. Samsung's Arguments

Samsung challenged claims of the '035 and '951 as obvious in light of Koyanagi and Alexander, and claims of the '226 as obvious in light of Koyanagi and Cooke. Appx736; Appx3803; Appx6514. Samsung also contended that all those claims were obvious in light of Bertin and Cooke. Appx736; Appx3803; Appx6514. Samsung's evidence included expert testimony from Dr. Stanley Shanfield, who has more than 35 years of experience in semiconductor fabrication, circuit design, and electronic module design and fabrication, including experience designing stacked chip modules using through-silicon vias. Appx1284-1288(¶¶8-19).

For the Koyanagi-based grounds, Samsung showed, with Dr. Shanfield's testimony and other evidence, that a skilled artisan "would have been motivated to apply Koyanagi's universal 3D integration teachings

to vertically stack the components of an FPGA-based reconfigurable computer system," such as the systems taught in Alexander and Cooke.[4] Stacking dies, as Koyanagi taught, would achieve "miniaturization, lower power consumption, and large-scale integration," which are well-known benefits and important for FPGA-based systems. Appx760.[5] It would also solve a well-known speed-degradation problem. *Id.*[6]

For Koyanagi and Alexander, Samsung showed (with evidence including Dr. Shanfield's testimony) that a skilled artisan would have expected success stacking an FPGA die (as Alexander taught) with memory and microprocessor dies (as Koyanagi taught) using "Koyanagi's universal 3D integration teachings" because both references disclose using the same 3D integration scheme: through-silicon vias and solder bumps on the die surfaces, as shown in both references' figures. Appx761;

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[4] Appx760; Appx1326-1327(¶104); Appx3820; Appx4363-4364(¶78); Appx6531; Appx7123-7124(¶68); *see also* Appx1330(¶110); Appx4367(¶82); Appx7126(¶72).

[5] *See also* Appx1326-1327(¶104); Appx3820; Appx4363-4364(¶78); Appx6531-6532; Appx7123-7124(¶68); Appx1883-1884.

[6] *See also* Appx1327(¶¶105-06); Appx3820; Appx4363-4364(¶78); Appx6531-6532; Appx7123-7124(¶¶68-69); Appx1840; Appx1844; Appx1846.

Appx1327-1329(¶¶107-108); Appx3821; Appx4364-4366(¶¶79-80); Appx1844-1845; Appx1840-1841.

For Koyanagi and Cooke, Samsung showed (with evidence including Dr. Shanfield's testimony) that a skilled artisan would have "been motivated to apply Koyanagi's broadly applicable 3D integration scheme to integrate the FPGA, memory, and microprocessor components of Cooke's system into a compact single 3D chip." Appx6533-6534; Appx7126(¶72). A skilled artisan would have understood that Koyanagi's vertical interconnections, which enable "large data bandwidth in vertical data transfer," would serve Cooke's goals of achieving "nearly instantaneous reconfiguration" of the FPGAs and shifting the configuration data in the memory planes "into the FPGA function in a single cycle." Appx6532; Appx7124-7125(¶70); Appx1844; Appx1850; Appx1856(2:47-49).

For Bertin and Cooke, Samsung likewise showed (with evidence including Dr. Shanfield's testimony), that a skilled artisan "would have been motivated to combine the teachings of Bertin and Cooke … to create a stacked processor module with an FPGA, memory, and processor to provide improved performance and area-efficiency." Appx788;

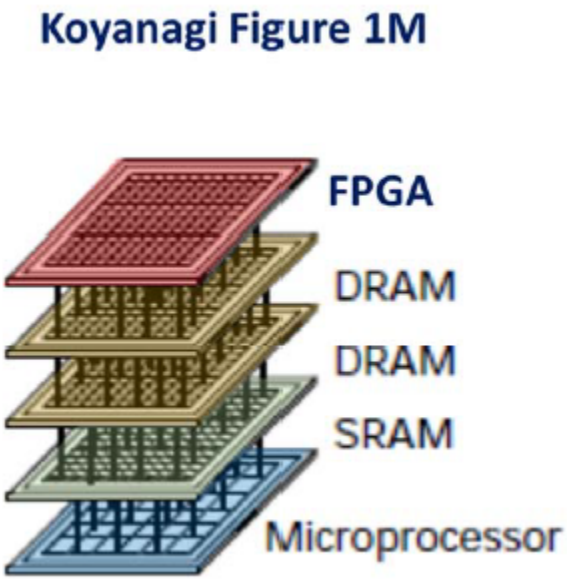
Appx1363(¶158); Appx3847-3848; Appx4391(¶117); Appx6552; Appx7147(¶101). "[A] POSITA would have understood that Bertin teaches stacking FPGAs with other chips, because an FPGA is a logic chip, and Bertin expressly discusses stacking a logic chip with other chips." Appx789; Appx1364(¶161); Appx3848; Appx4392-4393(¶120); Appx6553; Appx7148(¶104); Appx1872(7:16-34). Vertically stacking "the functional components of the FPGA-based reconfigurable computer system described in Cooke according to Bertin's 3D integration teachings" would "achieve high system packing densities, [and] high performance inter-chip and intra-chip communication and heat dissipation," for improved performance and area-efficiency over prior-art 2D reconfigurable systems. Appx790; Appx1365(¶163); Appx3849-3850; Appx4393-4394(¶122); Appx6554-6555; Appx7149(¶106); Appx1869(2:61-65).

Samsung and Dr. Shanfield also explained that a skilled artisan "would have found it obvious to try stacking the functional components of Cooke as taught by Bertin, and would have had a reasonable expectation of success doing so, because Cooke suggests a stacked system and Bertin provides broadly applicable, detailed teachings for stacking different processors, memories and logic chips such as FPGAs." Appx791;

Appx1366(¶165); Appx3850-3851; Appx4394-4395(¶124); Appx6555; Appx7150(¶108).

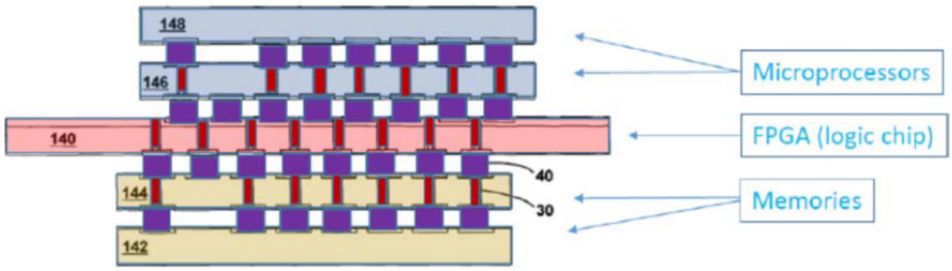
For all combinations, Samsung demonstrated (with evidence) why a skilled artisan would have combined references and how the combinations rendered each claim obvious Appx763-788; Appx791-812; Appx3824-3847; Appx3851-3871; Appx6534-6552; Appx6555-6574.

Samsung's submissions included illustrations to show how a skilled artisan would modify or combine prior art. The illustration below, titled "Koyanagi Figure 1*M*" (for modification), is Koyanagi Figure 1(a), modified so that "the exemplary top DRAM die is replaced with an FPGA die."



Appx1329-1330(¶109); Appx4366-4367 (¶81); Appx7125-7126(¶71). Another illustration, below, titled "Bertin in View of Cooke Annotated Figure 22A," below, shows Cooke and Bertin's teachings combined.

Bertin in view of Cooke
Annotated Figure 22A



Appx1365-1366(¶164) ("*This* stacking of Cooke's FPGA-based reconfigurable computer system according to Bertin's 3D integration teachings is illustrated in the annotated version of Bertin's Figure 22 below…").[7] Samsung's submissions used illustrations to summarize points that were also explained with words. Contrary to Arbor's suggestions (at 4, 13-14, 18-19, 44-45), Samsung did not argue—and the Board did not find—that the illustrations themselves rendered any claims obvious. *See infra* pp.20, 62-63.

[7] *See also* Appx4394(¶123) (same); Appx7149-7150(¶107) (same); *see* Appx790-791; Appx3850; Appx6554-6555.

2. The Board Institutes and Concludes All Challenged Claims are Unpatentable.

a. Institution Decisions

Finding "a reasonable likelihood that [Samsung] would prevail," the Board instituted proceedings for all three Samsung petitions. Appx946-947; Appx3995; Appx6702-6703. Arbor's description of the institution decisions is inaccurate.

The Board did not "ben[d] over backwards," or "rel[y] on [Samsung's] figures to institute." OpeningBr.11, 13, 18-20. It relied on a thorough review of the evidence, and treated the illustrations as illustrations, nothing more. *E.g.*, Appx937-946; Appx3986-3995; Appx6694-6702.

The Board did not "shift" the "burden of persuasion" when it commented on the petitions' merits. OpeningBr.3, 33. The IPR statute and precedent require preliminary consideration of the merits at institution. *See* 35 U.S.C. §314(a) (institution prohibited unless the Board finds "reasonable likelihood" of invalidating "at least 1" claim); Appx910 (*Fintiv* factor 6 is "other circumstances, that impact the Board's exercise of discretion, *including the merits*").

Nor did the Board did "act as an advocate for [Samsung's] possible renewed motion to stay [in district court]." OpeningBr.12. Board precedent requires consideration of co-pending court proceedings. Appx910 (*Fintiv* factors 1-5). The Board appropriately considered that the district court was likely to grant a stay and delay trial because the petitions made "a strong showing of unpatentability," and the Board instituted all three IPRs. Appx910-912; Appx3966-3968; Appx6674-6676; *see also* Appx979; Appx4028; Appx6736.

b. Final Decisions

After full briefing, a hearing, and (in the '226 IPR) supplemental briefing, Appx6934, the Board found all challenged claims unpatentable on all asserted grounds—*i.e.*, each challenged claim was invalid at least twice over.[8] Appx58-59; Appx127; Appx179; *supra* p.9 (chart).

The Board considered all the arguments Arbor renews on appeal. Arbor argued that the proposed combinations would have required "undue experimentation," but Arbor relied on testimony that not only "d[id]

[8] For the '035 patent, the Board also concluded that Alexander anticipates claims 1, 5, and 7, and Alexander in view of admitted prior art renders claims 9, 13, and 15 obvious. Appx19; Appx26. Arbor does not challenge those rulings on appeal.

not support" its argument but "indicate[d]" the opposite—that skilled artisans "readily would have been able to connect different die circuits together." Appx33-36; Appx 96; Appx101-103; Appx160-162 (Koyanagi+Alexander or Cooke); Appx49-50; Appx116-117; Appx172-173 (Bertin+Cooke). The Board credited Samsung's "detailed explanation of *how* Koyanagi and Alexander would have been combined … and *why* a POSITA would have been motivated to combine them." Appx35; *see also* Appx37-39; Appx102-104; Appx161-162 (Koyanagi+Alexander or Cooke); Appx49-50; Appx116-117; Appx173 (Bertin+Cooke). And the Board observed that Arbor's patents "provide[] the same level of detail with respect to stacking chips using conductive vias" as the prior art, which "suggests an artisan of ordinary skill readily knew how to connect FPGA and memory to a microprocessor." Appx35-37; *see also* Appx50-51; Appx104-106; Appx119-120.

The Board also rejected Arbor's argument that "thermal issues" weighed against obviousness. Appx42-45; Appx56-57; Appx109-113; Appx123-125; Appx159; Appx162; Appx171-174. The "many short vertical conductive vias," taught in prior art, reduce power consumption and improve heat removal, thus providing "further motivation" to combine,

"with an expectation that the combination would be successful." Appx42-43; *see also* Appx55; Appx111-112; Appx122-123; Appx162; Appx173-174.

For the '226 patent's means-plus-function claims, the Board rejected Arbor's argument that the structure and function must be found together in one prior-art reference, stating "we consider what the *combined* teachings of the references would have suggested to those of ordinary skill in the art." Appx163; *see also* Appx172. The Board found each combination (Koyanagi+Cooke and Bertin+Cooke) taught the means-plus-function elements. Appx164-165; Appx172; Appx175.

Arbor requested Director review, arguing that the same panel cannot issue institution decisions and final decisions. Appx1256-1257; Appx4307-4308; Appx7067-7068. The petitions were denied. Appx181-183.

B. Xilinx Separately Challenges and Invalidates Claims of the '226, '951, '035, and '214 Patents.

1. Xilinx's Challenges

Xilinx filed four IPR petitions challenging claims of the '035, '214, '226, and '951 patents.[9] *See* Appx17293-17379 ('035); Appx9079-9139 ('214); Appx13026-13107 ('951); Appx21769-21850 ('226). Xilinx contended that all challenged claims were obvious primarily in view of Zavracky, Chiricescu, and Akasaka. *Id.*[10]

Most of these references' details are not important for this appeal because Arbor does not challenge their teachings or the motivation to combine them. Instead, Arbor says the Board "relied on hindsight to shortcut the reasonable expectation of success inquiry." OpeningBr.5 (issue two). But that is not so.

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[9] If this Court affirms the Board's decisions in the Xilinx matters, then all challenged patent claims in all appellate cases would be affirmed as invalid. This is because Xilinx's petitions challenge a superset of the patent claims at issue in the Samsung petitions.

[10] Xilinx's exhibits were largely identical in its IPRs. Where the same document appears in multiple IPR records, this brief cites to one copy (preferably the version that Arbor cites in its opening brief) to avoid unnecessary duplication in the appendix.

Xilinx presented the Board with substantial evidence about the reasonable expectation of success of the asserted combinations. Xilinx supported its combinations with the expertise and detailed explanation of Professor Paul Franzon of North Carolina State University, who had over a decade of 3D circuit experience prior to these patents' purported invention date. Appx17922-18134 (at 17934-17936). Dr. Franzon explained the long history of 3D circuit development, what was well known in the art, the known advantages of stacked chips, and particulars of the references here. Appx17943-17957; Appx18004-18016. Dr. Franzon testified regarding motivation to combine and the reasonable expectation of success for 36 pages with dozens of citations to supporting evidence. Appx18017-18053. He further rebutted Arbor's specific technical attacks on reasonable expectation of success in detail. Appx19596-19657 (at 19599-19629).

a. Xilinx Showed How and Why a Skilled Artisan Would Have Combined Zavracky, Chiricescu, and Akasaka.

Xilinx's prior art combinations drew generally on:

- **Zavracky** for disclosing various dies stacked as a 3D circuit, including a processor, memory, and a programmable array;

- **Chiricescu** for citing Zavracky and disclosing a 3D chip with a FPGA that has on-chip memory for configuration information; and
- **Akasaka** for disclosing many parallel die-to-die connections via holes between dies, thus making the chip run faster.[11]

Arbor (at 21-23) does not describe the key teachings from this prior art. We review those briefly for context to help this Court evaluate the Board's finding of reasonable expectation of success in combining these teachings. (Arbor does not challenge these teachings, but only challenges the reasonable expectation of success in combining the teachings.)

Zavracky (Appx9865-9892) discloses 3D chips. Appx9880-9884. Its chips have "programmable logic arrays" stacked with "memory" and "microprocessors." Appx9889(12:14-40). These layers are connected through "via holes" that "can be placed anywhere."[12]

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[11] *See* Appx9100-Appx9108 ('214 petition); Appx13048-13056 ('951 petition); Appx17315-17322 ('035 petition); Appx21790-21797 ('226 petition) Appx18004-18011 & Appx18017-18032 (expert testimony); Appx203-215 ('214 decision); Appx303-315 ('951 decision); Appx417-428 ('035 decision); Appx545-554 ('226 decision).

[12] Appx9885(4:4); Appx9886(6:46); Appx9890(13:46-63).

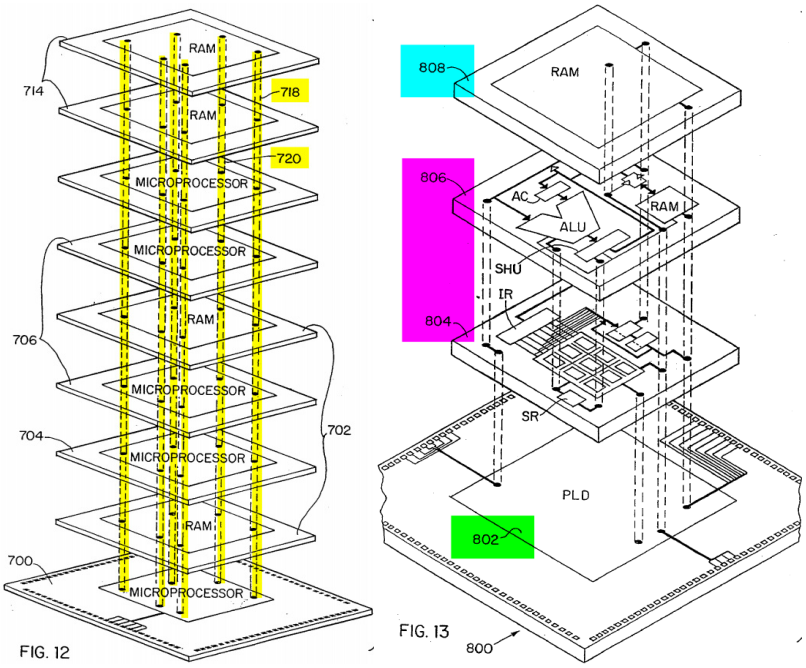
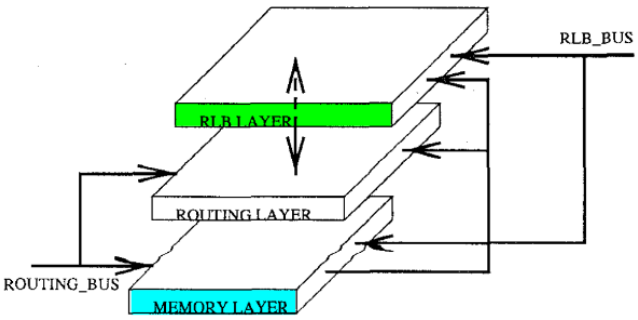


FIG. 12 FIG. 13

Appx21790-21791 ('226 petition highlighting memory (*blue*), microprocessors (*purple*), programmable logic (*green*), and vias (*yellow*)).[13]

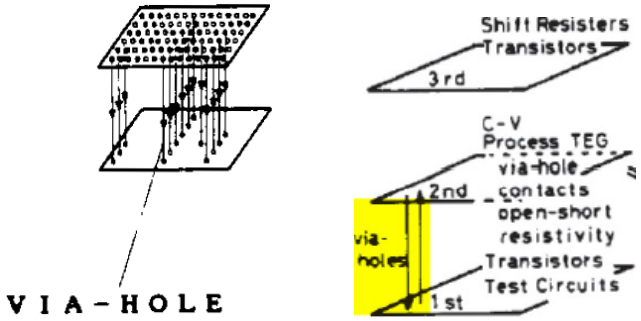
Chiricescu (Appx9893-9896) teaches a 3D chip with FPGA programmable logic and memory layers. Appx9893. It cites Zavracky by name as enabling 3D chips with "vertical metal interconnections (i.e., interlayer vias) placed anywhere on the chip" and uses that technology. *Id.*



[13] *See also* Appx9100-9101; Appx13048-13050; Appx17315-17316.

Appx21792-21793 ('226 petition highlighting memory (*blue*) and FPGA (*green*)).[14]

Akasaka (Appx18237-18259) teaches having lots of "via holes" throughout the chip—rather than bunching all the vertical wires in one place—to enable "parallel processing" between the chip layers. Appx18239. Akasaka shows many examples, including in devices with "three stacked active layers." Appx18237-18238, Appx18241-18243.



Appx21793 ('226 petition); Appx25361; Appx25425.[15]

Xilinx presented the Board with seven detailed reasons *why and how* a skilled artisan would have been motivated to combine these references and had a reasonable expectation of success in doing so.[16] Arbor's

[14] *See also* Appx9102-9103; Appx13050-13051; Appx17317-17318.

[15] *See also* Appx9103-9104; Appx13051-13052; Appx17318.

[16] Appx9104-9108 ('214 petition); Appx13052-13056 ('951 petition); Appx17319-17322 ('035 petition); Appx21794-21797 ('226 petition); Appx Appx18017-18032 & Appx19599-19607 (expert testimony).

"hindsight" objection below is a cloaked challenge as to whether Xilinx presented substantial evidence to the Board, and we address it in §I.B of the Argument section *infra*.

b. Xilinx Showed How and Why a Skilled Artisan Would Have Combined Trimberger.

Arbor's other technical issue concerns Trimberger, which addresses the means-plus-function claims in the '226 patent for configuring the FPGA "within one clock cycle."

Trimberger (Appx9920-9926) teaches how to connect the FPGA and memory to update the entire FPGA configuration in a single clock cycle. Each FPGA "configuration cell" is connected to a "memory cell." Appx9924. Every FPGA configuration cell is then loaded at the same time from the connected memory cell, thereby achieving one-cycle FPGA configuration. Appx9920; Appx9925.

More specifically, potential "configurations of the FPGA are stored in on-chip memory." Appx9920. The "memory is distributed around the chip, and accessible so that the entire configuration of the FPGA can be changed in a single cycle." *Id.* In Trimberger's model, potential configurations are stored in "memory planes (figure 1) [reproduced below]." *Id.*

During "single cycle" FPGA configuration, "all bits in the logic and interconnect array are updated simultaneously from one memory plane." *Id.*

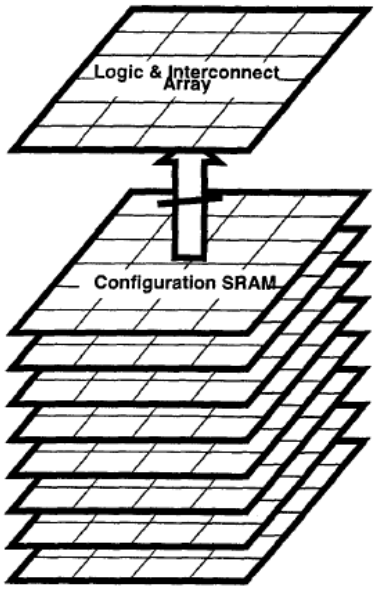


Figure 1. Time-Multiplexed FPGA Configuration Model

Appx9921; *see also* Appx21823 ('226 petition); Appx17358-17360; Appx25437-25439.

Xilinx cited Trimberger's teaching of sufficient connections between memory and FPGA to update the FPGA in one clock cycle, *i.e.*, to inform the skilled artisan of "how to direct the connectivity permitted by Akasaka's distributed contact points, and Zavracky and Chiricescu's teachings of contact points anywhere."[17] Xilinx presented the Board with

[17] Appx18042(¶254) & Appx19617-19618(¶46) (expert testimony); *see also* Appx21829-21833 (petition); Appx22138-22175 (at 22167-22168) (reply).

five detailed reasons *why and how* a skilled artisan would have been motivated to combine Trimberger with a reasonable expectation of success.[18] Arbor does not dispute most of these reasons, and we rebut Arbor's specific objections in §II.B of the Argument section *infra*.

2. The Board Institutes and Concludes All Challenged Claims are Unpatentable.

The Board instituted Xilinx's four petitions.[19] After full briefing and oral argument, the Board issued four written decisions, spanning 390 pages of detailed analysis. Appx184-573.

On the issues raised in this appeal, the Board made a "full review of the record" and explained why it found Xilinx's evidence to be "persuasive" as to reasonable expectation of success. *See, e.g.*, Appx226-230 (Board discussing expected success in detail in '214 decision); Appx331-350 (same for '951 decision), Appx436-497 (same for '035 decision);

[18] Appx21823-21825 (petition); Appx18037-18044 & Appx19614-19623 (expert testimony). *See also* Appx17358-17359 (petition).

[19] Because Arbor's opening brief is not clear on this point, and to avoid any confusion: none of Arbor's "prejudgment" or "annotated figures" arguments (*e.g.*, at 3, 4, 11-14, 33) relate to the Xilinx cases. Arbor does not identify any purported defect with the Xilinx institution decisions.

Appx553-571 (same for '226 decision). The Board walked through Xilinx's evidence and Arbor's counter-arguments in detail. *Id.* It quoted examples of Dr. Franzon's "credible" testimony (*e.g.*, at Appx441-442), contrasted this to the unsupported testimony by Arbor's expert Dr. Souri (e.g., at Appx464-465), and noted the "many references" (*e.g.*, at Appx438) that supported the expectation of success.[20] The Board analyzed Xilinx's evidence of other successful stacked devices, including those taught in Dr. Franzon's own prior work (*e.g.*, at Appx468). The Board extensively cited the record to support its findings, *see, e.g.*, Appx436-44, and found that Xilinx "persuasively shows ample evidence of a reasonable expectation of success" in the combination. Appx442.[21]

The Board also explained in detail why it found Arbor's counter-arguments "unavailing" in the face of Xilinx's evidence. Appx440-457. At bottom, Arbor misrepresented the record. The Board repeatedly found that "Patent Owner mischaracterize[d] Petitioner's showing," *e.g.*, that

[20] *See also*, *e.g.*, Appx236 ("Dr. Franzon's testimony in this regard more credible than Dr. Souri's testimony. Dr. Franzon's testimony is based on specific descriptions of references consistent with his opinion, whereas Dr. Souri's testimony does not provide evidentiary support"); Appx209; Appx214-215; Appx257; Appx328; Appx445; Appx550.

[21] *See also, e.g.*, Appx226-230; Appx331-350; Appx553-571.

the "record does not support [Arbor's] argument," that Arbor "throughout its briefing … confuses issues," that Arbor "exploits [a] difference of use in the terminology to confound issues," and that Arbor's "conflation represents the opposite of Dr. Franzon's testimony and Petitioner's showing."[22] As to the specific references, the Board found, *e.g.*, that Arbor had described Zavracky "contrary" to its actual teachings, that "there [was] no support for [Arbor's] line of argument" regarding Chiricescu, and that Arbor "describe[d] Akasaksa's teachings inaccurately."[23]

As to the combination with Trimberger, the Board found "persuasive," and "clearly stated," the following argument from Xilinx that flowed from Dr. Franzon's analysis:

> The wide configuration data port (i.e., the place through which the configuration data is transferred to each of the configuration logic cells in the FPGA) using the contact points, is provided by Zavracky in combination with Chiricescu and Akasaka (and in particular, the "thousands or several tens of thousands of via holes are present in these devices" taught by Akasaka), and Trimberger (for the "memory access port" that

[22] Appx446; Appx449 n.19; Appx455; Appx467-468; *see also, e.g.*, Appx220; Appx222-223; Appx230; Appx249; Appx271; Appx329; Appx342-344; Appx346; Appx543-544; Appx552-553.

[23] Appx437; Appx445; Appx463; Appx468; Appx471-472; Appx485; *see also, e.g.*, Appx222-223; Appx243-244; Appx250; Appx271; Appx328; Appx330; Appx336; Appx345; Appx346-347; Appx349; Appx350; Appx369; Appx370; Appx384; Appx552-553.

> connects to the configuration data "memory plane"). As discussed, integration of Trimberger's teachings yields the claimed function of "reconfiguring the programmable array within one clock cycle."

Appx566 (citing Appx21832-21833; Appx569); *see also* Appx489-497. The evidence showed "how" and "why" the skilled artisan would have made the combination—*i.e.*, a skilled artisan would use "Trimberger['s teaching] of instantly switching to a new configuration with bit lines for a memory plane read simultaneously from configuration memory" Appx566 (citing Appx21829-21831 & Appx9925)—implemented with Akasaka's many die-to-die connections in the Zavracky+Chiricescu 3D chip containing memory and FPGA), and the reasons they would do it included to obtain known fast FPGA reconfiguration benefits with known structures. Appx18037-18044 & Appx19614-19623 (expert testimony); Appx21823-21825 & Appx17358-17360 (petitions).

Dr. Franzon had described how the teachings of each reference would be applied in a modified final combination. In contrast, the Board faulted Arbor for treating the references "in isolation." Appx566. After careful review, the Board found all challenged claims to be unpatentable.

SUMMARY OF THE ARGUMENT

I.A. Arbor's proposed rule for obviousness of means-plus-function claims is inconsistent with precedent, and misquotes the Board. Consistent with §103's text and *KSR*, precedent holds that a *combination* of references can render claims obvious, with no additional requirement to show that individual references disclose entire claim elements. The Board properly rejected Arbor's argument, without ever suggesting Arbor was correct.

I.B. Substantial evidence supports the Board's rulings that the '226 patent's means-plus-function claims are obvious. The Board permissibly credited Samsung's and Xilinx's evidence showing that a skilled artisan would have been motivated to combine prior-art teachings with a reasonable expectation of success, in the manner of the claims—including the structures corresponding to the means-plus-function elements. Arbor understates the record evidence and the Board's reasoning, and fails to reckon with the substantial-evidence standard of review.

II. Arbor's "hindsight" attacks on the Board's decisions are undeveloped and unsound. Arbor suggests a lack of detail in the prior art, Samsung's and Xilinx's submissions, and the Board's reasoning, but

those are little more than Arbor's simple disagreement with the results. Arbor's arguments are wrong, and fail to reckon with the standard of review. The Board specifically addressed each of Arbor's arguments, and permissibly and separately credited Samsung's and Xilinx's evidence and arguments showing why and how a skilled artisan would have been motivated to combine prior-art teachings and in doing so would have obtained what Arbor later claimed, with a reasonable expectation of success.

III. It does not violate the APA or due process, or otherwise show "bias," where the same panel of APJs renders both institution and final decisions.

Ethicon rejects Arbor's arguments, is binding precedent, and was correctly decided. Applying Supreme Court precedent to reject Arbor's APA argument, *Ethicon* explains that institution is *adjudicatory*, not prosecutorial within the meaning of 5 U.S.C. §554. That a decision involves discretion does not make it "prosecutorial."

Ethicon likewise applies Supreme Court precedent to reject Arbor's due process/bias argument, on two levels. First, even if institution were prosecutorial, it is not a due process violation to combine prosecutorial

and adjudicatory functions. Second, however characterized, it is not a due process violation or evidence of "bias" for an adjudicator to decide institution and the final merits. Courts at every level of the judiciary regularly make similar preliminary and final rulings on the merits. Adjudicators have a presumption of honesty and integrity. "Bias" requires a showing of exposure to *ex parte* information or a conflict of interest, which are both absent here.

This Court should affirm.

ARGUMENT

Standard of Review

This Court reviews the Board's factual findings for substantial evidence and legal conclusions *de novo*. *Ethicon*, 812 F.3d at 1028. Motivation to combine, reasonable expectation of success, and what a prior-art reference discloses are all factual questions and thus reviewed for substantial evidence. *IXI IP, LLC v. Samsung Elecs. Co.*, 903 F.3d 1257, 1262 (Fed. Cir. 2018). Under the substantial-evidence standard, this Court "do[es] not reweigh the evidence," and the question is not whether substantial evidence may have supported the appellant's view of the facts, "but instead whether such evidence supports the findings that were

in fact made." *Regents of Univ. of Cal. v. Broad Inst.*, 903 F.3d 1286, 1294 (Fed. Cir. 2018).

I. The Board Properly Analyzed Obviousness of the '226 Patent Claims With Means-Plus-Function Elements.

Arbor does not dispute any of the Board's claim constructions. OpeningBr.25-26. For the '226 patent, Arbor **(A)** asks this Court to invent a special obviousness rule for means-plus-function elements, and **(B)** disputes whether substantial evidence supports the Board's findings. OpeningBr.31-41. Both arguments are unsound.

A. Obviousness of Claims With Means-Plus-Function Elements Does Not Require that a Single Reference Disclose the Structure and Function Together.

Arbor contends (at 3, 33-34) that the Board's decisions invalidating the '226 claims contravened "black letter law" to the effect that a claim with a means-plus-function element is only obvious if a *single* prior-art reference discloses the corresponding structure *and* function together. Arbor's proposed rule is unsupportable, contrary to precedent, and would distort the obviousness test.

Obviousness compares prior art to "the claimed invention *as a whole*." 35 U.S.C. §103. The analysis is "expansive and flexible," *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 415, 419 (2007), and considers prior

art "not only for what it expressly teaches, but also for what it fairly suggests." *Bradium Techs., LLC v. Iancu*, 923 F.3d 1032, 1049 (Fed. Cir. 2019) (quoting *In re Baird*, 16 F.3d 380, 383 (Fed. Cir. 1994)). Consistent with *KSR*, this Court's precedent holds that obviousness does not require specific disclosures of entire individual claim limitations in individual prior-art references. Rather, "it is *sufficient* that a [skilled artisan] would have been motivated to combine the prior art in a way such that the *combination* discloses the claim limitations." *Fleming v. Cirrus Design Corp.*, 28 F.4th 1214, 1222 (Fed. Cir. 2022); *Bradium*, 923 F.3d at 1050 (Obviousness "cannot be overcome by attacking references individually where the rejection is based upon the teachings of a combination of references."); *Ormco Corp. v. Align Tech., Inc.*, 463 F.3d 1299, 1307 (Fed. Cir. 2006) (similar); *In re Sovish*, 769 F.2d 738, 742-43 (Fed. Cir. 1985) (similar).

The presence of means-plus-function elements does not change that analysis. Sections 103 and 112(f) (as §112 ¶6) were enacted together in 1952. Neither provision's text or legislative history suggests special obviousness rules for claims with means-plus-function elements. Section 112(f) was "enacted … in response" to the Supreme Court's 1946 *Halliburton* decision. *Warner-Jenkinson Co., Inc. v. Hilton Davis Chem. Co.*,

520 U.S. 17, 27-28 (1997). It simply allows patentees to claim structures indirectly by describing the structure in the specification and using the means-plus-function format to claim it: "[a]n element in a claim for a combination may be expressed as a means … for performing a specified function without the recital of structure … and such claim shall be construed to cover the corresponding structure … described in the specification and equivalents thereof." 35 U.S.C. §112(f). For example, a patentee can *either* claim "a nail configured to hold a picture to a wall," or claim "means for holding a picture to a wall" if the specification describes a nail used for that purpose. There is no reason to treat the two picture-nail claims differently for obviousness.

Arbor's citations are not to the contrary. Arbor (at 34) cites the dissent in *McGinley v. Franklin Sports, Inc.*, 262 F.3d 1339 (Fed. Cir. 2001), which *Fresenius USA, Inc. v. Baxter Int'l, Inc.*, 582 F.3d 1288 (Fed. Cir. 2009) quotes in part. *See also* Appx163; Appx567. Setting aside the oddity of deriving "black-letter law" from a dissent, both opinions merely reiterate what §112(f) explicitly says: means-plus-function elements are *limited* to the corresponding *structure* and equivalent structures.

Fresenius affirmed nonobviousness of means-plus-function claims where the challenger had "neither identified" the corresponding structure "nor compared it to the structures present in the prior art." 582 F.3d at 1299. *Fresenius* explained that "*a structural analysis is required* when means-plus-function limitations are at issue," and "a challenger who seeks to demonstrate that a means-plus-function limitation was present in the prior art must prove that the corresponding structure—or an equivalent—was present in the prior art." *Id.* at 1299.

Fresenius quoted the passage from *McGinley*'s dissent that Arbor quotes: "the invalidating prior art must disclose not simply a means for achieving the desired function, but rather the particular structure recited in the written description corresponding to that function, or an equivalent thereof." *Id.* (quoting *McGinley*, 262 F.3d at 1361 (Michel, J., dissenting)). Like *Fresenius*, the *McGinley* dissent states only that the challenger must show that "prior art" discloses the corresponding structure; neither opinion suggests disclosure of structure and function must be in a single reference.

Arbor misstates the record when it says (at 34) "the Board acknowledged this legal requirement." *See also* OpeningBr.3 (Board "acknowledged it was improper to do this type of mix-and-matching"); OpeningBr.29 (similar). In reality, the Board acknowledged *Arbor's argument*, before *rejecting* that argument as incorrect. Appx567. The Board explained that *Fresenius* did not support Arbor's "assertion of impropriety in finding structure and function in an asserted combination based on the *combined* teachings of references." *Id.*; Appx163 (same). And "no inference [could] be made" from the *McGinley* dissent because that case involved single-reference obviousness. Appx567-568; *see also* Appx163.

After rejecting Arbor's proposed rule, the Board conducted the analysis precedent requires. It required petitioners to prove that the claimed *structures* or equivalents were themselves obvious, and it "consider[ed] what the combined teachings of the references would have suggested to those of ordinary skill in the art." Appx163; *see also* Appx172; Appx567-568. *See Fleming*, 28 F.4th at 1222 ("[I]t is *sufficient* that a [skilled artisan] would have been motivated to combine the prior art in a way such that the *combination* discloses the claim limitations.").

B. Substantial Evidence Supports the Board's Findings in the '226 Patent IPRs.

Arbor's remaining arguments concerning the '226 patent's means-plus-function limitations reargue facts and disregard the substantial-evidence standard.

1. Substantial Evidence Supports the Board's Findings in the Samsung IPRs.

Samsung proved that the '226 patent's claims with means-plus-function limitations (claims 13, 22, and dependents) were obvious twice over: in light of **(1)** Koyanagi and Cooke, and **(2)** Bertin and Cooke. *See* Appx160-165; Appx172-176. Arbor's contrary arguments are unsound. OpeningBr.35-37.

As just explained, *supra* §I.A, Arbor is wrong to argue (at 35) "black letter law prohibits mismatching of structure and function." And as the Board properly noted, Arbor's argument misapprehends Samsung's arguments and the Board's reasoning. Appx164 (Arbor's argument is "not commensurate with" Samsung's arguments); Appx172-173 ("the combination … would have taught the wide configuration data port … [that] would perform the function described"). Neither Samsung nor the Board "mismatch[ed]" one reference's structure with another's function. Samsung showed how and why a skilled artisan would combine Koyanagi

with Cooke, and Bertin with Cooke, with a reasonable expectation of success. Appx6531-6534; Appx7123-7125(¶¶68-70); Appx7126(¶72) (Koyanagi+Cooke); Appx6552-6555; Appx7147(¶101); Appx7148(¶104); Appx7149(¶106); Appx7150(¶108) (Bertin+Cooke). The Board credited Samsung's evidence, and found the *combinations* each taught the claimed structures. *E.g.*, Appx161-162; Appx164-165; Appx172-173.

Arbor argues (at 35) "substantial evidence does not support the Board's finding that replacing Cooke's single chip FPGA reconfiguration structure with a stacked module having thousands of interconnections" teaches the means-plus-function claim limitations. None of Arbor's three arguments demonstrates error.

First, Arbor argues (at 35-36, quoting *McGinley* dissent) that Cooke's structure for reconfiguring the FPGA is different from the '226 claims' corresponding structure. That argument repackages Arbor's misstatement of means-plus-function precedent (addressed above). To be sure, Samsung argued the function of reconfiguring a programmable array in one clock cycle was well-known in the art and disclosed in Cooke. *See* Appx6538; Appx6559. But Samsung argued, and the Board found, that prior-art *combinations* taught the claims, including the claimed

structures. *See* Appx160-164; Appx172-175 (decision); Appx6538-6540; Appx6559-6561 (petition); Appx6838-6842; Appx6850-6852 (reply); Appx2963; Appx2983 (demonstratives). Obviousness "cannot be overcome by attacking references individually where the rejection is based upon the teachings of a combination of references." *Bradium*, 923 F.3d at 1050.

Second, Arbor is wrong to assert (at 36) the Board "failed to explain why or how a POSITA would have destroyed Cooke's single-chip FPGA structure," and "ignored Arbor's argument that it would not have been obvious to employ Koyanagi's or Bertin's vertical interconnections."

Citing evidence and briefing, the Board found Samsung provided "detailed explanation[s]" of "how" and "why" a skilled artisan would have combined Koyanagi with Cooke and Bertin with Cooke. Appx161-162; Appx173. Samsung explained that skilled artisans would understand stacking Cooke's components using Koyanagi's or Bertin's 3D integration teachings with vertical interconnections would "achieve[] the well-known benefits of 'miniaturization, lower power consumption, and large-scale integration'" and "solve[] [the] well-known problem" of speed degradation. Appx6531-6532 (quoting Appx1883-1884); Appx1840; Appx1844;

Appx1846; Appx7123-7124(¶68); *see also* Appx6554-6555 (stacking would improve performance and area-efficiency and achieve high-performance communication); Appx7149(¶106). Samsung also explained why a skilled artisan would have expected the combinations to succeed and achieve Cooke's goal of near-instantaneous FPGA reconfiguration. Appx6531-6534; Appx6554-6555; Appx7123-7126(¶¶68-72); Appx7148-7150(¶¶104, 106-108). The Board agreed that "Koyangi and Cooke *collectively* evidence a reasonable expectation of success in arriving at the claimed invention" because the combination "maintain[s] the large bandwidth connection taught by Cooke through the 3D integration with contact points on the surface of the dies, as taught by Koyanagi." Appx162; Appx172 (skilled artisan would have combined Bertin and Cooke, and the combination "would have taught a wide configuration data port" that performs the claimed function).

Arbor's reference to "destroy[ing] Cooke's single-chip structure" (at 36) ignores that obviousness is about combining prior-art teachings, not physically combining embodiments. *See Allied Erecting & Dismantling Co. v. Genesis Attachments, LLC*, 825 F.3d 1373, 1381 (Fed. Cir. 2016);

In re Etter, 756 F.2d 852, 859 (Fed. Cir. 1985) (en banc) (physical combinability is "basically irrelevant."); *KSR*, 550 U.S. at 415, 419 (obviousness test is "flexible," and "cannot be confined … by overemphasis on … explicit content of issued patents."). Samsung's evidence and arguments—which the Board appropriately credited—explained how a skilled artisan would "integrate" Cooke's components into "Koyanagi's broadly applicable 3D integration scheme." Appx157 (quoting Appx6533-6534); *see also* Appx6554 (like Koyanagi, "Bertin's 3D integration teachings" are "designed to universally 'accommodate different chip sizes and structures.'").

And far from stacking "unidentified" components of Cooke, OpeningBr.36, Samsung's petition identified Cooke's FPGA, memory, and microprocessor components, and illustrated *how* they would be stacked using Koyanagi's or Bertin's 3D integration teachings. Appx6533; Appx6553-6555. The Board did not "ignore" Arbor's arguments. *See* Appx158-160; Appx171-172 (summarizing Arbor's arguments). It considered them and was permissibly unpersuaded. Appx160-164; Appx172-175.

Third, the Board *did* articulate how Samsung's proposed combinations taught the "wide configuration data port" structure. OpeningBr.36-

37 (arguing otherwise). The Board credited Samsung's evidence and arguments that the Koyanagi+Cooke and Bertin+Cooke combinations would each have taught the "wide configuration data port." *See* Appx161-162; Appx164; Appx172-173.

The Board's reasoning and cited evidence refute Arbor's contention that Samsung failed to identify connected "cells." Arbor's reference to Cooke's FPGA "be[ing] cut up and reformed into a stacked module" (at 37) again confuses combining prior-art teachings with physically combining prior-art embodiments. *Etter*, 756 F.2d at 859. The Board appropriately credited Samsung's showing that a skilled artisan "would have understood the shifting of configuration data stored in memory into the FPGA in a single cycle …, with memory cells containing configuration bits [] connected in parallel to the logic cells of the FPGA die using the interconnections." Appx171 (citing Appx6945; Appx1998-1999); *see also* Appx158; Appx164; Appx175; Appx1854; Appx1856(2:30-31) (Figure 8B showing "cells" in the shared memory stack).

In sum, Arbor fails to show error.

2. Substantial Evidence Supports the Board's Findings in the Xilinx IPRs.

Xilinx also showed that the challenged '226 means-plus-function claims, including the structure of "a wide configuration data port and contact points formed throughout the area of the first [IC] die element and another [IC] die element," Appx537-538; Appx541, and corresponding functions, were obvious in view of teachings from Zavracky+Chiricescu+Akasaka and Trimberger. *See* Appx21823-21838 (petition); Appx565-570 (decision).

Xilinx presented substantial evidence as to the "why" and "how" of the combination and the expected success. Appx21823-21825 (petition); Appx18040-18044 & Appx19614-19623 (expert testimony). For "why," Xilinx showed that the skilled artisan would have sought out the combination in view of known problems, including to fix a recognized "bottleneck" of "high configuration time of an FPGA."[24] Xilinx also showed that the skilled artisan would have sought the combination to solve specific already-recognized problems "for a wide-range of applications requiring ultra-fast configuration of a FPGA" including "image target recognition"

[24] Appx21824 (citing Appx18041(¶252)).

where the need for "single clock cycle" FGPA reconfiguration was already well-known.[25] Xilinx also presented evidence that the skilled artisan would have sought the combination to improve Trimberger's goal of one-cycle configuration "by providing faster interconnects" and because "routing" would be easier with "reduced wirelength" in the combined 3D chip.[26]

For "how," Xilinx showed the Board that it was well-known to reconfigure an FPGA in a single clock cycle by connecting configuration cells with memory cells, and expert witness Dr. Franzon cited other prior art references besides Trimberger (including Cooke, Ong, and Tau) that provided this teaching.[27] Xilinx cited evidence identified from Dr. Franzon (including from his own prior work) that "the POSITA would also have expected success in directing [the 3D stack's] known area-wide interconnections for a particular purpose in re-programming the FPGA

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[25] Appx21824 (citing Appx18029-18030(¶235) & Appx18040-18041(¶¶251-252) (citing Appx23784-23793 (at 23785) ("one clock cycle"))).

[26] Appx19615-19617(¶¶44-45) Appx19619-19621(¶¶48, 52); *see also* Appx493-496 (Board crediting evidence as to same).

[27] Appx17991(¶145), Appx17994(¶157), Appx17997(¶169), Appx18040-18044(¶251, ¶¶255-256).

in a clock cycle."[28] Dr. Franzon cited third party "examples where similar integrations were successful" and showed that a skilled artisan would have modified Akasaka's multiple parallel connections, to carry signals as taught in Trimberger for the FPGA reconfiguration information.[29]

Xilinx and Dr. Franzon presented still further reasons to combine, including that a skilled artisan would want to use Trimberger's block memory "for the predictable benefit of supporting FPGA applications" in the chip stack of the other references, and Dr. Franzon gave three sub-reasons why. Appx18037-18040(¶¶247-249). Arbor does not challenge these additional showings on appeal.

Arbor dislikes those explanations and largely ignores them—but they address motivation to combine and likelihood of success, they are not conclusory, and they constitute substantial evidence. Arbor also largely ignores the substantial evidence standard of review, and instead repeats the attorney arguments that Arbor made below, which the Board was not obligated to accept.

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[28] Appx21825 (citing Appx18043-18044 (citing Appx23344-23356 (expert's prior work))).

[29] *See* Appx18043-18044; Appx19614-19623.

First, Arbor focuses (at 37-41) on Trimberger alone and does so with a myopic view of Trimberger's teachings. But Xilinx's challenge was not a single-reference anticipation challenge; it was a *multi*-reference *obviousness* combination challenge. The Board found that:

> The Petition persuasively shows that ["one clock cycle" means-plus-function] limitation[] is taught, not by Trimberger's teachings regarding the "single memory access port" that provides access to configuration memory[] alone, but rather in combination with the description in Trimberger of instantly switching to a new configuration with bit lines for a memory plane read simultaneously from configuration memory[] and with Akasaka's teaching of thousands or tens of thousands of via holes[].

Appx566. Arbor's arguments in this appeal ignore the Board's reasoning. As it did below, Arbor (at 37-41) on appeal focuses entirely on the single physical implementation of Trimberger's "single memory access port," and not on the *combination* of *teachings*. And just as the Board found below, Arbor's arguments on appeal again fail as they "relate … to the teachings of Trimberger *in isolation*, rather than in combination with the teachings of the art in combination." Appx566.

Second, even as to Arbor's attacks (at 38-41) on Trimberger in isolation, Arbor's arguments all center on an unstated assumption that obviousness must be analyzed based on a physical combination of prior art

rather than a combination of the art's teachings. That assumption is contrary to law. *Etter*, 756 F.2d at 859. It was entirely acceptable for the Board to conclude that the teaching of using sufficient connections to allow passage of each bit of reconfiguration data at the same time (to permit reconfiguration in a single cycle), along with the other prior art teachings, would have been obvious—and the substantial evidence described above certainly supported it. The Board was not required to stitch the particular physical structures of the prior art together.

Third, Arbor's argument (at 38-41) that Trimberger's "memory access port" does not provide the required structure[30] is misplaced, and suggests that Arbor does not understand the combination Xilinx proposed. Appx21832-21833 (petition); Appx22164-22168 (reply). As Dr. Franzon testified:

> Zavracky, Chiricescu, Akasaka combination already has a memory and an FPGA. It is already connected via a wide-area distributed set of interconnections as taught in Akasaka. One of the relevant teachings from Trimberger is in how to use those interconnections, i.e., to have sufficient interconnections to be able to update all of the logic cells in one clock cycle.

[30] Arbor again misrepresents the record below when it claims at the bottom of OpeningBr.40 that "Xilinx acknowledged this very fact" but then quotes *Arbor*'s misleading briefing.

Appx19617-19618(¶46); *see also* Appx18042(¶254) ("Trimberger's teaching [includes] how to direct the connectivity permitted by Akasaka's distributed contact points, and Zavracky and Chiricescu's teachings of contact points anywhere.").[31] The Board understood the combination, even if Arbor does not. Appx566.

Fourth, far from Arbor's assertion (at 39) that Trimberger's teachings are "mutually exclusive" with the rest of the combination, Xilinx and Dr. Franzon presented evidence that the skilled artisan would have *sought* the combination because of the advantages of the combined teachings.[32] The combination realized Trimberger's model (shown at Appx9921 & Appx19617) and enabled signals to travel shorter distances in the vertical direction, thereby achieving faster speed. Appx19615-19617(¶¶44-45). The inclusiveness of the teachings is supported by substantial evidence, and Arbor's assertions to the contrary appear to be tied

[31] Further, the question is not whether Trimberger has a "corresponding structure" for the claimed means, but whether the '226 means-plus-function claims as a whole (with the corresponding structure from the '226 specification) would have been obvious from all that the prior art taught and suggested. *See supra* §I.A.

[32] Appx21823-21825; Appx22173-22174; Appx19615-19617(¶¶44-45) Appx19619-19621(¶¶48, 52); *see also* Appx493-496, Appx565 & Appx568-569 (Board crediting evidence as to same).

to its improper legal view that references must be physically plugged together.

Fifth, and relatedly, Arbor is wrong (at 40) to fault the Board for correctly stating that Arbor never showed the "location of Trimberger's on-chip memory [to be] necessary in some way to Trimberger's teachings." That is, Trimberger does not limit its teachings to only apply in a 2-D chip, as opposed to a 3D chip stack, as Dr. Franzon "explained credibly." Appx492-493 (citing Appx19615-19616(¶¶44)); Appx569.

Finally, Arbor is wrong (at 41) because the Board did not "disregard" Arbor's evidence about how Trimberger achieves one-clock-cycle reconfigurations. Rather, the Board was allowed to evaluate the full teachings of the prior art; the Board was not required to stop with Arbor's artificially narrow view of Trimberger's physical embodiment—and substantial evidence supported the Board's reasoning. *See, e.g.*, Appx18040-18044; Appx19614-19623.

II. None of the Board's Final Decisions Are "Tainted by Hindsight."

Arbor next attacks all seven decisions as relying on "hindsight." OpeningBr.42-46 (Samsung decisions); OpeningBr.47-52 (Xilinx decisions). In each decision, the Board applied the correct legal standards,

addressed all of the parties' arguments, and explained with detailed reasoning and evidentiary citations why it found each claim invalid. Arbor's "hindsight" arguments mainly allude to arguments Arbor made below and assert that the Board was wrong to reject them, which is generally insufficient to preserve an argument for appeal. *Arunachalam v. IBM Corp.*, 989 F.3d 988, 998-99 (Fed. Cir. 2021) (quoting cases); *Monsanto Co. v. Scruggs*, 459 F.3d 1328, 1341 (Fed. Cir. 2006). To the extent preserved, the arguments are meritless.

A. Arbor Fails to Show Error in the Samsung Final Decisions.

Arbor does not address the Board's rulings that Alexander anticipates claims 1, 5, and 7 of the '035 patent, or that Alexander and admitted prior art render claims 9, 13, and 15 obvious. *See* Appx736; *supra* p.21 n.8. Those rulings should be affirmed in all events. *Engel Indus., Inc. v. Lockformer Co.*, 166 F.3d 1379, 1383 (Fed. Cir. 1999) (arguments not in opening brief are unpreserved).

Arbor challenges only obviousness grounds where Koyanagi or Bertin is the primary reference. OpeningBr.42-46. There, Arbor mismatches arguments and decisions. Arbor cites arguments it made about the '226 patent (at 42-43), then (at 44) cites the Board's decision on the '035 patent

as "[r]ejecting *these* arguments." That is no mere technicality, as different combinations were asserted against each patent: Koyanagi and Alexander against the '035 patent, and Koyanagi and Cooke against the '226 patent. *See also, e.g.*, OpeningBr.44 (comparing '226 claim construction (Appx147) with '035 obviousness ruling (Appx29-31; Appx42)). More broadly, Arbor offers only general, unsupported criticisms of Samsung's arguments, prior art, and the Board's decisions, while failing to reckon with the substantial-evidence standard.

First, Samsung did not fail to explain why a skilled artisan would have stacked an FPGA with other components. Arbor alleges a lack of detail in the evidence, arguing (at 42) that Samsung only "cited references that generically disclose stacking dies … and references that disclose FPGAs," and (at 42-43) that this case is "[j]ust like" *TQ Delta, LLC v. Cisco Sys., Inc.*, 942 F.3d 1352 (Fed. Cir. 2019), because (Arbor argues) Samsung's expert did "not explain how" prior-art teachings "would or could be combined … to reach the claimed invention." Arbor's descriptions are false.

The prior art is not so "generic" or limited, as explained above, *supra* pp.10-14, and as the Board found. For example, the Board found

Koyanagi's technology is "agnostic as to the dies it connects," Appx37, and made unchallenged findings that Alexander does not just "disclose FPGAs," but **(1)** *anticipates* some of Arbor's claims, and **(2)** discloses *stacking* FPGA dies and *connecting* them with through-silicon vias. Appx13; Appx17; Appx38.

And unlike *TQ Delta*, as the Board explained, Samsung provided "detailed explanation of *how*" to combine specific references, and "*why* a POSITA would have been motivated to combine them." Appx35; *see also* Appx37-39; Appx102-104; Appx161-162 (Koyanagi+Alexander or Cooke); Appx49-50; Appx116-117; Appx172-175 (Bertin+Cooke); *see also supra* pp.14-18. Samsung explained the motivation to combine Koyanagi and Alexander—for "increased data speed, lower power, miniaturization, and other benefits"—and why the combination had an expectation of success—because "both references 'depict the use of through-silicon contacts …' and 'both illustrate vertical stacking of integrated circuit dies and depict solder bumps that are distributed on the surface of the dies." Appx30-31 (citing Appx760-762; Appx1840; Appx1844); *see also* Appx90-91 (citing Appx3823-3824); Appx157-158 (similar explanation for Koyan-

agi+Cooke, quoting Appx6533-6534). Samsung likewise explained in detail why a skilled artisan would have been motivated to combine Bertin and Cooke and expected success. Appx48-49; Appx116-117; Appx170; Appx790-791; Appx3849-3851; Appx6554-6555.

Second, the Board considered and properly rejected Arbor's arguments (at 43-44) that a skilled artisan could not combine prior-art teachings without "undue experimentation," and that Samsung "slapped together" references or otherwise "oversimplified" the technology. *See* Appx35; Appx37-39; Appx102-104 (Koyanagi+Alexander); Appx161-162; Appx171 (Koyanagi+Cooke); Appx49-50; Appx116-117 (Bertin+Cooke). The Board explained, for each combination, why those arguments were unpersuasive, including specifically rejecting Arbor's characterizations of "slapping together" references. *See* Appx34-39; Appx49-55; Appx100-103; Appx116-117; Appx160-164; Appx171-172.

For all the challenged claims, Samsung specifically addressed interconnections, showing that a skilled artisan would connect die elements using through-silicon vias and contact points, *as taught in the prior-art references*. Appx32-33; Appx47-49; Appx91-93; Appx115-116; Appx156-158; Appx169-170. No "undue experimentation" was necessary

because skilled artisans "readily would have been able to connect different die elements together," and would have considered "which connections you want a [through-silicon via] connecting to" based on the circuit one has in mind. Appx34-35; Appx3455(82:3-19); *see also* Appx49-50; Appx101-102; Appx116-117; Appx160-161; Appx173.

Moreover, as the Board noted, Arbor's patents do "not portray or particularly describe connections between microprocessor die 64 and the other dies … other than to show generic contacts in Figure 4." Appx36. The Board permissibly inferred that lack of detail suggests "an artisan of ordinary skill readily knew how to connect FPGA and memory to a microprocessor." Appx35-36; *see also* Appx50-51; Appx105-106; Appx119-120; Appx684. Arbor generally cannot fault the prior art for lacking details that its own patent also lacks. *See Alcon Research, Ltd. v. Apotex, Inc.*, 687 F.3d 1362, 1369 (Fed. Cir. 2012); *Merck & Co. v. Teva Pharms. USA, Inc.*, 395 F.3d 1364, 1373-74 (Fed. Cir. 2005).

Third, Arbor's repeated references to the "wide configuration data port" (at 43-46) concern only the '226 patent. No other challenged patent claims a "wide configuration data port." The "wide configuration data port" appears only in figure 5 and a paragraph of the specification.

Appx144. The Board rejected Arbor's attempts to import Figure 5's "wide configuration data port" into other patents, noting it "does not pertain to the microprocessor die or to any claim limitation," Appx36-37; Appx104-105, and observing that it is "merely a box without any description." Appx37; Appx105. For the '226 patent, the Board rejected Arbor's attempt to import what details there were in Figure 5 into the claims. Appx145-146. And as addressed above, *supra* pp.43-49 (§I.B.1), Samsung's submissions and the Board's decisions sufficiently explained why the '226 patent's means-plus-function claims are obvious, including identifying connected "cells" and explaining how prior art taught the "wide configuration data port" structure.

Arbor misstates the record when it contends (at 44) that Samsung argued for connecting *Cooke's* FPGA to *Koyanagi's* DRAM. Rather, Samsung argued that a skilled artisan would stack "components of Cooke's reconfigurable processor system" (including memory, *e.g.*, DRAM) according to Koyanagi's teachings. Appx6533.

Nor is it true, as Arbor argues (at 46), that "Samsung fought against the Board's ultimate construction of 'wide configuration data port' …be-

cause Samsung had never showed how that art would have been combined even in that level of detail." Again, Arbor's level-of-detail criticisms are unfounded, and substantial evidence supports the Board's findings that the '226 patent's means-plus-function claims—as ultimately construed—were obvious. *Supra* pp.43-49. And as to Samsung's arguments below, the Board properly understood that Samsung sought a construction that "clarifie[d] the die elements described as connected in parallel" in the context of the '226 patent. Appx143 (quoting Appx6941). Samsung argued that there should be no reference to "cells" of the third integrated circuit die element because the '226 patent "does not refer to the 'wide configuration data port' connecting *cells* on the *memory die*" to FPGA cells. Appx6941-6942.

Finally, Arbor's criticisms of illustrations (at 44-45; *see also* OpeningBr.4, 13, 18, 20) lack substance. Notwithstanding Arbor's epithets (*e.g.*, "cartoons," "made-up"), litigants properly use illustrations to communicate facts and arguments. R.C. Hughey, *Effective Appellate Advocacy Before the Federal Circuit: A Former Law Clerk's Perspective*, 11 J. APP. PRAC. & PROCESS, 401, 421 (2010) (quoting former Chief Judges Markey and Michel on visual aids in briefs). Courts properly do the same,

sometimes generating their own illustrations. *E.g.*, *United States v. Rentz*, 777 F.3d 1105, 1109 (10th Cir. 2015) (en banc) (Gorsuch, J.) (sentence diagram); *Sandifer v. U.S. Steel Corp.*, 678 F.3d 590, 592 (7th Cir. 2012) (photograph). Samsung neither treated the illustrations as prior art in themselves, nor relied on illustrations *alone* to show obviousness. They were visual aids, and only part of the explanation of how a skilled artisan would combine prior-art teachings.[33] The Board neither misunderstood nor misused the illustrations, *e.g.*, Appx47-48 (figures "represent how petitioner combines the relevant teachings"), nor relied on illustrations alone to find the claims obvious, as Arbor argues (at 4, 44-45). In sum, Arbor's "hindsight" accusations are unfounded.

B. Arbor Fails to Show Error in the Xilinx Final Decisions.

Arbor does not point to any "hindsight" affecting the Xilinx IPRs. OpeningBr.47-52. To the extent Arbor truly raises a hindsight argument from the Xilinx IPRs, expert Dr. Franzon explained the motivation to combine the asserted references, he provided full reasoning, and the

[33] Appx1329-1330(¶109); Appx1365-1366(¶164); Appx4366-4367(¶81); Appx4394(¶123); Appx7125-7126(¶71); Appx7149-7150(¶107).

Board credited it.[34] On a substantial-evidence standard of review, that results in affirmance.

The substance of Arbor's arguments (at 47-52) is not about any hindsight, but rather further quibbles with the substantial evidence of a reasonable expectation of success, while ducking the relevant legal standard. Arbor again focuses on the wrong issue by alleging difficulties in the physical combinability of the systems disclosed in the references.[35] But "'[t]he test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference,' but rather whether 'a skilled artisan would have been motivated

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[34] *See See* Appx18017-Appx18047, Appx19599-19607, Appx19614-19632 (expert testimony); Appx9104-9108, Appx9129-9130 ('214 petition); Appx13052-13056, Appx13087-13089, Appx13094-13095 ('951 petition); Appx17319-17322, Appx17358-17360, Appx17366-17367 ('035 petition); Appx21794-21797, Appx21823-21825 ('226 petition); Appx211-230 ('214 decision); Appx303-350, Appx363-372 ('951 decision); Appx417-428, Appx489-497 ('035 decision); Appx545-570 ('226 decision).

[35] Examples of Arbor falling into its physical combinability error include: **(1)** "which cells in a memory die would be connected in parallel to which cells of Chiricescu's FPGA" (at 47); **(2)** "how Akasaka's several tens of thousands of via holes would or even could be interconnected with FPGA circuitry of Chiricescu, Trimberger, or Alexander" (at 48-50) (note: "tens of thousands" not in claim language); and **(3)** "mov[ing] Chiricescu's or Trimberger's on-chip memory from an FPGA to the separate off-chip stacked memory die" (at 51-52) (note: "off-chip" not in claim language).

to combine the teachings of the prior art references to achieve the claimed invention.'" *Allied*, 825 F.3d at 1381 (collecting cases) (internal citations omitted). And Xilinx showed that, as noted immediately above.

Further, even Arbor's technical quibbles are wrong. *First*, Arbor claims (at 47-48) "neither Xilinx nor the Board identified which cells in a memory die would be connected in parallel to which cells of [the] FPGA in order to reach the 'wide configuration port' of Arbor's Patents [sic]." That is not so. The only patent claims with a "wide configuration port" are in the '226 patent.[36] And Xilinx's challenge included the teachings from Trimberger, which teaches that each FPGA cell is connected in parallel to a memory cell. Appx9924 ("configuration *cells* … are backed by … memory *cells*"); *see also* Appx21831-21833 (petition); Appx22167-22168 (reply); Appx22258-22373 (at 22275(18:12-20)) ("Trimberger is describing memory as a memory plane which is comprised of *cells* that is instantaneously swapped to update programmable array configuration *cells* … the CLB configuration *cells* are connected to memory *cells*, and

[36] A "wide configuration data port" is only relevant to the '226 means-plus-function claims 13 and 22 (through the Board's construction) and their dependents. There is no "wide configuration data port" in any claim of the '035, '214, or '951 patents.

the configuration *cells* are part of the logic and interconnect array"); Appx22279-22280(22:20-23:3) ("Trimberger gives … the direction. [I]f you want to reconfigure in one clock cycle, you need to make sure that all of the memory *cells* are connected to the configuration and logic *cells*, … on a one-to-one basis between *cells*."). The Board discussed Xilinx's argument as to the wide configuration data port and found it "persuasive." Appx566. Arbor's appeal just ignores the relevant arguments, evidence, and findings.

Second, Arbor alleges (at 48) that there was not "any explanation or showing" as to "how" Akasaka's wide-area connections "could be interconnected with … Chiricescu, Trimberger, or Akasaka." But Arbor's argument **(1)** again is about physical combination and does not reflect the combination of *teachings*, **(2)** does not reflect the claim language,[37] and **(3)** is wrong because Xilinx and Dr. Franzon *did* provide extensive evidence as to "how" the teachings of the references would be combined. *See, e.g.*, Appx21796-21797 (petition); Appx17652-17689 (at Appx17679-

[37] The claims have no requirement as to a specific number of connections, and the Board recognized that "[Arbor] also agrees that the number of interconnects is not critical to the claimed invention." Appx440; Appx22305-22306(48:9-49:9).

17682) (reply rebutting Arbor's "how" arguments); Appx19599-19607(¶¶13-28) (Dr. Franzon collecting evidence). In particular, Akasaka taught wide-area interconnections. Xilinx's evidence showed how third parties had successfully made such a combination. Appx17681-17682. Xilinx also showed how Arbor *conceded* that distributed contact points between dies was well known. Appx17680-17681. Further, Dr. Franzon showed four examples where such connections between dies had been described in the art, including from his own work. Appx17680 n.6. The Board properly credited the "ample evidence of a reasonable expectation of success." Appx442. *See also* Appx226-230; Appx331-336; Appx551-554.

Third, Arbor repeats (at 49-52) a misleading technical argument regarding "off-chip memory access" that Arbor also made below. But **(1)** substantial evidence supports the Board's findings (see *supra*); **(2)** the Board was not required to accept Arbor's incorrect view of the evidence; **(3)** Arbor's arguments again are about physical combination, which is not the proper inquiry; and **(4)** the Board detailed in a long footnote why and

how Arbor's characterization of the evidence was a "conflation [that] represents the opposite of Dr. Franzon's testimony and Petitioner's showing," Appx449. *See also* Appx229-230; Appx252-253; Appx342-343.

A few additional words may be helpful as to this last point about Arbor's "conflation" of the evidence. In short, Arbor tried to use different meanings of the word "chip" to try to sow confusion. The evidence was that the word "chip" sometimes referred to an entire 3D chip module (e.g., Appx19615-19616(¶44), discussing 3D chips) and sometimes referred to a die/chip within the 3D module (*e.g.*, Appx17943-17944 n.2, where Dr. Franzon quoted dictionary evidence showing that "'die' and 'chip' are sometimes used interchangeably"). The Board noted how Arbor tried to "exploit this difference of use in the terminology to confound issues." Appx449 n.19.

Arbor now repeats (at 49-52) the same misleading argument about "off-chip access" that it presented below.[38] But the Board understood the

[38] For example, Arbor quotes (at 49) Dr. Franzon's testimony that was about "off-chip access" from the "3D *module*." Appx17678 (summarizing evidence of same and citing Appx12868 at Appx12886(71:16-72:11)). But Arbor inserts language (at 49) in brackets into the quote ("[e.g., off-chip memory separate from the FPGA *die*]"), which changes the meaning of the testimony. Arbor then shows (at 50) a different quote where Arbor's counsel asked Dr. Franzon whether an element was found on "the same

issues, recognized the dual meaning of the term "chip" and the context of the testimony, and explained in detail why it rejected Arbor's "conflation" of facts. Appx449 n.19.[39] The Board was well within its rights to reject Arbor's misleading presentation below, and accept Xilinx's substantial evidence showing obviousness.

In short, Arbor does not argue or show any actual "hindsight" and Arbor's actual arguments fail against the substantial evidence standard.

III. Arbor's Arguments Against Permitting the Same Panel to Render Institution and Final Decisions Are Foreclosed by *Ethicon* and Meritless in Any Event.

Arbor argues that the same panel cannot legally render the institution decision and final decision in the same IPR. Arbor contends that

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die" within the "stack." In that context, Dr. Franzon referred to the different die as "off-chip" with respect to the first die. Appx12879(42:15-43:3). Arbor then combines (at 50) the two statements—that were about two different things—to argue that "the Board's conclusion rested on a mistaken understanding of "off-chip." But the Board understood the issues, saw through Arbor's misrepresentation, and noted that Arbor was "conflating" the evidence. Appx342; Appx449; Appx229-230.

[39] Similarly, Arbor repeatedly misstates (at 51-52) Xilinx's combination as "moving on-chip memory to a separate stacked memory die." Not only is this a misdirected physical combinability argument, but this was not even Xilinx's proffered combination and the Board understood that. Appx494 ("Petitioner does not propose "moving' Trimberger's on chip memory' … contrary to Patent Owner's argument")). *See also* Appx17683-17684 & Appx22174-22175.

arrangement combines prosecutorial and adjudicatory functions and creates "bias," violating the APA and due process principles. OpeningBr.52-69. Recognizing that *Ethicon* rejects those arguments, Arbor contends *Ethicon* was wrongly decided. *Ethicon* is binding precedent, forecloses Arbor's arguments, and was correctly decided. *See Mobility Workx, LLC v. Unified Patents, LLC*, 15 F.4th 1146, 1157 (Fed. Cir. 2021) (reaffirming *Ethicon*).

A. *Ethicon* Rejects Arbor's Arguments and Controls This Case.

Ethicon considered and rejected the same APA and due process arguments Arbor makes here.

First, *Ethicon* rejected the argument—which Arbor repeats some 40 times—that institution is a "prosecuting function" within the meaning of 5 U.S.C. §554(d)(2). 812 F.3d at 1030. Section 554(d)(2) provides in part that "[a]n employee or agent engaged in the performance of *investigative or prosecuting functions* for an agency in a case may not, in that or a factually related case, participate or advise in the decision, recommended decision, or agency review pursuant to section 557 of this title, except as witness or counsel in public proceedings."

Ethicon holds "[b]oth the decision to institute and the final decision are *adjudicatory* decisions and do not involve combining investigative and/or prosecutorial functions with an adjudicatory function." 812 F.3d at 1030. Institution "is directly analogous to a district court determining whether there is a 'likelihood of success on the merits' and then later deciding the merits of a case." *Id.; see id.* at 1030 n.3 (citing §554(d), noting "the APA imposes no separation obligation as to those involved in preliminary and final decisions.").

Second, *Ethicon* rejected Arbor's due process argument—both because institution is not prosecutorial, *and* because combining prosecutorial and adjudicatory functions in an administrative tribunal is not a due process violation. 812 F.3d at 1029-31; *see id.* at 1029 ("[W]here … there are no other separate procedural-fairness infirmities alleged, … assignment of the institution and final decisions to one panel of the Board does not violate due process."). *Ethicon* cited precedent rejecting similar arguments, *e.g.*, *Withrow v. Larkin*, 421 U.S. 35, 58 (1975), and noted "the Supreme Court has never held a system of combined functions to be a violation of due process, and it has upheld several such systems." 812 F.3d at 1029 (quoting treatise). *Ethicon* specifically addressed the "bias"

argument Arbor makes here. Under Supreme Court precedent, administrators have a "presumption of honesty and integrity." *Id.* at 1030 (quoting *Withrow*, 421 U.S. at 47). When an adjudicator forms an opinion based on a limited record early in the case, or when an agency "combin[es] the functions of initial decision and final disposition in the same Board panel," neither is evidence of bias. *Id.* at 1030-31 (citing *Withrow* and *Liteky v. United States*, 510 U.S. 540, 551 (1994)).

Ethicon sought *en banc* rehearing and certiorari. Both were denied. 826 F.3d 1366 (Fed. Cir. 2016), *cert. denied*, 137 S.Ct. 625 (2017). And in 2021, this Court applied *Ethicon* to reject "nearly identical challenge[s]" from another petitioner. *Mobility Workx*, 15 F.4th at 1157. The Court should do the same here. *Ethicon* binds panels, *Vas-Cath Inc. v. Mahurkar*, 935 F.2d 1555, 1563 (Fed. Cir. 1991), and rejects Arbor's arguments.

Arbor believes *Ethicon* is wrong, *e.g.*, OpeningBr.55 ("*Ethicon* should be overruled"), OpeningBr.62 ("The *Ethicon* Court Erred …"), but does not appear to dispute that *Ethicon* is binding precedent. Arbor quotes three post-*Ethicon* decisions (at 63) as if to suggest they are intervening authority. All three decisions predate *Mobility Workx*; none undermine *Ethicon*'s holdings.

St. Regis Mohawk Tribe v. Mylan Pharms. Inc., 896 F.3d 1322, 1327 (Fed. Cir. 2018), merely observed that IPRs resemble "agency enforcement action[s]" in some ways. *St. Regis* considered whether tribal sovereign immunity applied to IPRs. The Court observed that IPRs are a "hybrid proceeding" resembling private civil litigation in some ways, and agency enforcement actions in other ways. The Court reasoned that precedent in the latter category provided a better analogy for the immunity issue before the Court. 896 F.3d at 1326-30. *St. Regis* neither called institution decisions "exercise[s of] *prosecutorial* discretion" as Arbor suggests, OpeningBr.63, nor considered §554(d).

Cuozzo Speed Techs., LLC v. Lee, 579 U.S. 261, 279 (2016), merely remarked that IPRs and reexaminations "reexamine an earlier agency decision," which does not support Arbor's argument. Arbor contends (at 63) *Cuozzo* is "similar[]" to *St. Regis*, but as just explained, *St. Regis* does not support Arbor either. Like *St. Regis*, *Cuozzo* did not consider §554(d) or suggest institution is prosecutorial.

Oil States Energy Servs., LLC v. Greene's Energy Grp., LLC, 138 S.Ct. 1365 (2018), likewise did not consider the issues Arbor raises. It

observed "the decision whether to institute inter partes review is committed to the Director's discretion," *id.* at 1371, but "discretionary" does not mean "prosecutorial." *See infra* §III.B.1.

B. *Ethicon* Was Correctly Decided.

In criticizing *Ethicon*, Arbor misreads statutes, relies on an unsupported analogy to criminal prosecutors, and ignores Supreme Court precedent discussed in *Ethicon*. Even if the Court entertains Arbor's criticisms, *Ethicon* was correctly decided.

1. *Ethicon* Correctly Rejects Arbor's Statutory Argument.

Arbor analogizes institution decisions to a criminal prosecutor filing charges. If there is any IPR analogue to a criminal prosecutor, it is the *petitioner*, not the Board. The petitioner chooses which claims to challenge on which grounds (*i.e.*, which charges to bring), it gathers evidence, and it presents charges and evidence to the agency in a petition. 35 U.S.C. §§311-312. The "petitioner is master of its complaint," and at institution the agency has no "discretion regarding *what* claims" to review. *SAS Institute v. Iancu*, 138 S.Ct. 1348, 1355, 1356 (2018). The Director (or delegate) considers the petition and any preliminary response, and can only choose between proceeding with the entire package of challenges

in the petition, or not proceeding at all. 35 U.S.C. §314(a); *SAS*, 138 S.Ct. at 1356.

As *Ethicon* correctly explains, institution decisions are essentially preliminary adjudications of the merits. 812 F.3d at 1030. They are no different from district judges' decisions whether to: **(a)** issue warrants, **(b)** detain criminal defendants before trial, **(c)** issue preliminary injunctions or TROs, or **(d)** hear declaratory judgment claims. They are no different from courts of appeals' decisions whether to: **(e)** grant a stay or injunction pending appeal, **(f)** grant rehearing en banc, or **(g)** stay a mandate pending certiorari. And they are no different from the Supreme Court's decisions whether to: **(h)** grant a stay or injunction pending review, or **(i)** grant certiorari. *See Withrow*, 421 U.S. at 56 n.24 ("[A]pproving the institution of proceedings is much like what judges do in ruling on demurrers or motions to dismiss.").

Arbor emphasizes (at 55, 63) the Director has "discretion" whether to institute. But not all "discretion" is *prosecutorial* discretion. In all nine examples above, the adjudicator exercises discretion while considering the case's merits, but does not exercise a "prosecutorial" function. The same is true of institution decisions. *See Withrow*, 421 U.S. at 56 (It is

"very typical for the members of administrative agencies to receive the results of investigations, to approve the filing of charges or formal complaints instituting enforcement proceedings, and then to participate in the ensuing hearings. *This does not violate the Administrative Procedure Act*, and it does not violate due process of law.").

Arbor cites no decision from any court that treats an agency's institution decision as "prosecut[orial]." Indeed, precedent addressing §554(d) only illustrates how far afield Arbor's arguments are. *Grolier v. FTC*, 615 F.2d 1215, 1220 (9th Cir. 1980) held that §554(d) may require an FTC ALJ's recusal from cases relating to those the ALJ had investigated in his former job as an FTC attorney-advisor. *Grolier* reasoned that §554(d) embodies two concerns: exposure to *ex parte* information, and "will to win" developed from working on the case *as an investigator*. *Id; see also In re Grolier, Inc.*, 87 FTC 179 (1976) (similar). If an IPR petitioner's attorney leaves private practice to become an APJ, then §554(d)(2) and conflict-of-interest rules would likely require recusal from IPRs related to that person's work in private practice. But those principles have no application to an APJ's continued participation in a case merely after rendering an institution decision.

Arbor emphasizes that the AIA charges the Director with institution decisions and the Board with final decisions. OpeningBr.54, 58-59 (citing 35 U.S.C. §§314(d), 318(a)). Because those statutes reference different actors, Arbor contends—with no further analysis or explanation—they implicitly wall the Director off from the Board and require "separate" decisionmakers.

Ethicon correctly rejected that argument. 812 F.3d at 1031 ("There is nothing in the statute or legislative history … indicating a concern with *separating* the functions of initiation and final decision."). The AIA and binding precedent make institution and final written decisions both ultimately the Director's decisions. The AIA assigns institution to the Director by default, 35 U.S.C. §314(a), but the Director can delegate to the Board, and has done so for institution decisions. 37 C.F.R. §42.4(a). And although the AIA assigns final written decisions to the Board, *United States v. Arthrex*, 141 S. Ct. 1970, 1987 (2021), holds that 35 U.S.C. §6(c) must permit the Director to review final decisions. 35 U.S.C. §6(a), moreover, defines the Board to include the Director.

Arbor gives up the game when it accepts the propriety of delegating institution decisions. Arbor insists (at 61 n.6) that "two *separate* entities,

under the supervision of the Director" must still "perform the *separated* institution and final written decision functions."[40] But Arbor has no support other than to circle back to insisting that the AIA requires "separate" actors for institution and final decisions. At bottom, Arbor is asking the Court to impose additional procedures beyond statutory requirements. *See Vt. Yankee Nuclear Power Corp. v. NRDC*, 435 U.S. 519, 525 (1978).

2. *Ethicon* Correctly Rejects Arbor's Due Process Argument.

As *Ethicon* explains (and Arbor ignores), *Withrow* rejects due process arguments based on **(a)** combining prosecutorial and adjudicative functions, and **(b)** the same adjudicator making preliminary and final merits decisions. 812 F.3d at 1029. "[T]he Supreme Court has never held a system of combined functions to be a violation of due process, and it has upheld several such systems." *Id.* (quoting 2 R.J. PIERCE, ADMINISTRATIVE LAW TREATISE, §9.9, p. 892 (5th ed. 2010)). Examples include

[40] Section 554(d)(2) explicitly "*does not apply* … "to the agency or a member or members of the body comprising the agency." That exemption plainly excludes the Director from the provision Arbor relies on, yet Arbor does not mention the exemption. The Court need not reach the issue, but to the extent 554(d)(2) "does not apply" when the Director acts through a delegate, as with institution decisions, that would be yet another reason why Arbor's statutory argument lacks merit.

Withrow; *Goss v. Lopez*, 419 U.S. 565 (1975) (due process requires a hearing before a student can be suspended, but the hearing can be informal and the principal can be investigator, prosecutor, and decisionmaker); *Marcello v. Bonds*, 349 U.S. 302, 311-14 (1955) (upholding combination of prosecution and adjudication); *id.* at 307-09 (distinguishing *Wong Sun* case Arbor cites); and *Richardson v. Perales*, 402 U.S. 389 (1971) (upholding combination of investigation and adjudication).

As Arbor ignores, Supreme Court precedent rejects the argument that "bias" results when adjudicators make preliminary decisions. *Withrow*, 421 U.S. at 50 n.16, 56; *Liteky*, 510 U.S. at 551 ("opinions held by judges as a result of what they learned in earlier proceedings" are "not … 'bias' or 'prejudice.'"); *Ethicon*, 812 F.3d at 1030 (quoting *id.*).

"Bias" generally requires a showing that "an adjudicator is exposed to unofficial, 'extrajudicial' sources of information," *Ethicon*, 812 F.3d at 1030, or has a conflict of interest such as "a pecuniary interest in the outcome" or "has been the target of personal abuse or criticism from the party before him." *Withrow*, 421 U.S. at 47. Arbor makes no such showing here. It only offers a quotation from *Tumey v. Ohio*, 273 U.S. 510

(1927), and an advocacy organization's statistics. OpeningBr.67-69. Neither shows bias.

Tumey does not hold that any possible "temptation" an adjudicator might feel is a due process violation. *Tumey* addressed a mayor's court where the mayor was **(a)** paid for convictions but not acquittals, and **(b)** responsible for the village's finances, which were funded in part by conviction fees. The problem was not "temptation" in the abstract, but the mayor-adjudicator's "direct, personal, substantial, pecuniary interest in reaching a conclusion against" one of the parties. 273 U.S. at 523. Neither *Tumey* nor any other authority bars preliminary and final decisions by the same adjudicator. *Cf. Mobility Workx*, 15 F.4th at 1152-55 (discussing *Tumey*).

Finally, Arbor's assertion that 84% of final written decisions invalidate at least one claim is misleading and not evidence of bias. That statistic omits cases where no final decision results (*e.g.*, because of settlement, dismissal, non-institution, or granting a motion to amend), and does not distinguish between decisions invalidating all claims, some claims, or only one. The PTAB reports that approximately 22-32% of

cases settle, and only 24% of petitions result in a final decision invalidating all challenged claims. USPTO, PTAB TRIAL STATISTICS, FY22 END OF YEAR OUTCOME ROUNDUP IPR, PGR at 10, 11 (2022), *at* https://www.uspto.gov/sites/default/files/documents/ptab__aia_fy2022_roundup.pdf. On a claim-by-claim basis, 76% of claims addressed in final decisions are ruled unpatentable, which is only 26% of all challenged claims. *Id.* at 13. Institution decisions, moreover, are not random. Institution only happens if **(a)** the petitioner is willing to pay tens of thousands in filing fees and accept estoppel for any upheld claims, 35 U.S.C. §315(e)(1), and **(b)** the Board finds a reasonable likelihood that at least one claim will be found invalid, *and* does not deny institution for other reasons. Even through Arbor's artificially narrow lens, 84% means the Board upholds *all* claims 16% of the time, notwithstanding an earlier belief that the evidence would likely lead to invalidation of one or more claims. Arbor may believe the PTAB invalidates too many claims, but that is a policy concern for Congress or the PTO, not a proper due process argument for this Court.

CONCLUSION

The Court should affirm.

March 1, 2023

Respectfully submitted,

/s/ Jeffrey Shneidman
(signed with permission)

Jeffrey Shneidman
FISH & RICHARDSON P.C.
One Marina Park Drive
Boston, MA 02210
(617) 542-5070

John Dragseth
FISH & RICHARDSON P.C.
60 South Sixth St., Suite 3200
Minneapolis MN 55402
(612) 335-5070

David M. Hoffman
Kenneth Darby
FISH & RICHARDSON P.C.
111 Congress Ave., Suite 810
Austin TX 78701
(512) 472-5070

Counsel for Xilinx, Inc.

/s/ John C. O'Quinn

John C. O'Quinn
F. Christopher Mizzo
William H. Burgess
KIRKLAND & ELLIS LLP
1301 Pennsylvania Ave, N.W.
Washington, D.C. 20004
(202) 389-5000

Meredith Zinanni
KIRKLAND & ELLIS LLP
300 North LaSalle
Chicago, IL 60654
(312) 862-2000

Counsel for Samsung Electronics Co., Ltd.

/s/ Eric Huang
(signed with permission)

James M. Glass
Eric Huang
QUINN EMANUEL URQUHART & SULLIVAN, LLP
51 Madison Avenue
New York, NY 10010
(212) 849-7000

Counsel for Taiwan Semiconductor Manufacturing Co., Ltd.

CERTIFICATE OF COMPLIANCE WITH TYPE-VOLUME LIMITATION

This brief complies with the type-volume limitations of the Federal Rules of Appellate Procedure and the Rules of this Court. According to the word processing system used to prepare it, the brief contains 13,848 words.

/s/ John C. O'Quinn